

# **PV SYSTEMS SECONDARY INJECTION PROTECTION TEST REPORT**

**Customer name - ABC Energy**

---

**REPORT NUMBER – SI-15381**

# PV SYSTEMS SECONDARY INJECTION PROTECTION TEST REPORT

## Client Information

Client Name	ABC Energy
Client Address	51 Frontview Hwy. Ringwood 3134
Contact Person	Jonathan Rose
Contact Phone Number	03 8663 2222



## Test Object : InteliPro Relay

### Summary Results

Test date: **01-Dec-17**

Test Performed by **John Steve**

Contact Number **0414000451**

Protection	Setting	Trip Time	Result
Over Voltage II	260V	2s	Pass
Under Voltage II	180V	2s	Pass
Over Frequency II	52Hz	2s	Pass
Under Frequency II	47.5Hz	2s	Pass
ROCOF	2Hz/s	1s	Pass
Vector Shift	8°		Pass
Prepared by: <b>John Steve</b> Bsc.Eng (Hons)			
Approved By: <b>Sean Senarathne</b> Bsc.Eng(Hons)			
Date	02-Jan-18		

**Note:**

1. Schematic Reference for testing DQ17-0298MEL3-02
2. External Trip Tested OK.
3. Light Indicators' Functions Tested OK.

## Test Object - Device Settings

**Substation/Bay:**

Substation:	PETER STEVENS MOTORCYCLES	Substation address:	
Bay:		Bay address:	

**Device:**

Name/description:	Intelipro/ Mains Decoupling relay	Manufacturer:	Comap
Device type:	Grid Protection	Device address:	
Serial/model number:	N/A		
Additional info 1:	Dara Switchboards		
Additional info 2:			

**Nominal Values:**

f nom:	50.00 Hz	Number of phases:	3
V nom (secondary):	400.0 V	V primary:	400.0 V
I nom (secondary):	70.00 A	I primary:	70.00 A

**Residual Voltage/Current Factors:**

VLN / VN:	1.732	IN / I nom:	1.000
-----------	-------	-------------	-------

**Limits:**

V max:	500.0 V	I max:	70.00 A
--------	---------	--------	---------

**Debounce/Deglitch Filters:**

Debounce time:	3.000 ms	Deglitch time:	0.000 s
----------------	----------	----------------	---------

**Overload Detection:**

Suppression time:	50.00 ms
-------------------	----------

## Test Object - Other RIO Functions

**CB Configuration**

Description	Name	Value
CB trip time	CB trip time	50.00 ms
CB close time	CB close time	100.00 ms
Times for 52a, 52b in percent of CB time	52a, 52b % of CB	20.00 %

## Test Object - Overcurrent Parameters

**General - Values:**

TimeTolAbs:	0.10 s	VT connection:	n/a
TimeTolRel:	10.00 %	CT starpoint connection:	n/a
CurrentTolAbs:	0.10 Iref		
CurrentTolRel:	5.00 %		
Directional:	No		

## Test Object - Distance Settings

### System parameters:

Line length:	5.000 $\Omega$	Line angle:	75.00 °
PT connection:	at line	CT starpoint:	Dir. line
Impedance correction	no		
1A/I nom:			
Impedances in primary values:	no		

### Tolerances:

Tol. T rel.:	5.000 %	Tol. T abs. -:	0.000 s
Tol. T abs. +:	50.00 ms	Tol. Z abs.:	50.00 m $\Omega$
Tol. Z rel.:	5.000 %		

### Grounding factor:

kL mag.:	1.000000	kL angle:	0.000000°
Separate arc resistance:	no		

### Zone Settings:

## Hardware Configuration

### Test Equipment

Type	Serial Number
CMC356	FK335L

### Hardware Check

Performed At	Result	Details
1/12/2017 3:20:47 PM	Passed	

### Analog Outputs

Test Equipment		Test Object		
Device	Connector	Display Name	Connection Terminal	
CMC356 V A FK335L	1	V L1-E		
	2	V L2-E		
	3	V L3-E		
	N			

### Binary/Analog Inputs

Test Equipment		Test Object		
Device	Connector	Display Name	Connection Terminal	
CMC356 FK335L	1+	Trip		
	1-			
	2+	Bin. in 1		
	2-			
	3+	Bin. In. 3		
	3-			
	4+	Bin. In. 4		
	4-			
	5+	Bin. In. 5		
	5-			
	6+	Bin. In. 6		
	6-			
	7+	Bin. In. 7		
	7-			
	8+	Bin. In. 8		
	8-			
	9+	Bin. In. 9		
	9-			
	10+	Bin. In. 10		
	10-			
	1	Bin. In. 11		
	2	Bin. In. 12		
	N			

### Binary Outputs

Test Equipment		Test Object		
Device	Connector	Display Name	Connection Terminal	
CMC356 FK335L	1+	Bin. Out 1		
	1-			
	2+	Bin. Out 2		
	2-			
	3+	Bin. Out 3		
	3-			
	4+	Bin. Out 4		
	4-			
	11	Bin. Out 5		
	12	Bin. Out 6		
	13	Bin. Out 7		
	14	Bin. Out 8		
	N			

### Analog DC Inputs

Test Equipment		Test Object		
Device	Connector	Display Name	Connection Terminal	
CMC356 FK335L	V+	V1		
	V-			
	I+	I1		
	I-			

### AuxDC Configuration:

### Test Module

Name:	OMICRON AuxDC Configuration	Version:	3.20
Test Start:	01-Dec-2017 15:21:14	Test End:	01-Dec-2017 15:21:16
User Name:	Lahiru Wijesinghe	Manager:	Shanaka
Company:	Dara Switchboards		

## Test Results

**Test State:**  
Test passed

## QuickCMC:

### Test Module

Name:	OMICRON QuickCMC	Version:	3.20
Test Start:	01-Dec-2017 15:21:37	Test End:	01-Dec-2017 15:24:56
User Name:	Lahiru Wijesinghe	Manager:	Shanaka
Company:	Dara Switchboards		

## Test Results

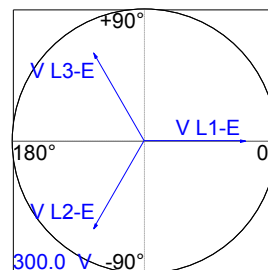
Title: Test 1

### Fault Calculator:

Table Inputmode	Parameters (All values are secondary)			
Direct	V L1-E	230.0 V	0.00 °	50.000 Hz
	V L2-E	230.0 V	-120.00 °	50.000 Hz
	V L3-E	230.0 V	120.00 °	50.000 Hz

### Generator Settings

V L1-E	230.000V	0.00°
V L2-E	230.000V	-120.00°
V L3-E	230.000V	120.00°



### Binary Inputs

Name	Slope	Time
Trip	0->1	62.119s
Bin. in 1	1->0	n/a

### Summary

1 tests passed, 0 tests failed, 0 tests not assessed  
Test passed

100.00% passed



## Under Voltage L1 (27P):

### Test Settings

#### General

No. of ramp states: 2  
 Total steps per test: 27  
 Total time per test: 81.000 s  
 No. of test executions: 1

Input Mode: Direct  
 Fault Type:

#### Ramped Quantities

V L1-E / Magnitude

#### Ramp States

Ramp	Ramp 1	Ramp 2
V L1-E	230.0 V 0.00 ° 50.000 Hz	200.0 V 0.00 ° 50.000 Hz
V L2-E	230.0 V -120.00 ° 50.000 Hz	230.0 V -120.00 ° 50.000 Hz
V L3-E	230.0 V 120.00 ° 50.000 Hz	230.0 V 120.00 ° 50.000 Hz
Force abs. Phases	Yes	No
Sig 1 From	230.0 V	200.0 V
Sig 1 To	230.0 V	175.0 V
Sig 1 Delta	0.000 V	-1.000 V
Sig 1 d/dt	-1.667 V/s	-333.3 mV/s
Bin. Out 1	0	0
Bin. Out 2	0	0
Bin. Out 3	0	0
Bin. Out 4	0	0
dt per Step	3.000 s	3.000 s
Ramp Steps	1	26
Ramp Time	3.000s	78.000s
Trigger	None	Bin
Trigger Logic		OR
Trip		0
Bin. In 1		X
Bin. In. 3		X
Bin. In. 4		X
Bin. In. 5		X
Bin. In. 6		X
Bin. In. 7		X
Bin. In. 8		X
Bin. In. 9		X
Bin. In. 10		X
Step back	No	No
Delay Time	0.000 s	0.000 s

### Test Module

Name: OMICRON Ramping  
 Test Start: 01-Dec-2017 10:51:33  
 User Name: Dileepa  
 Company: Dara Switchboards

Version: 3.20  
 Test End: 01-Dec-2017 10:52:34  
 Manager: Shanaka

## Test Results

### Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Trip	Ramp 2	Trip 1->0	V L1-E	180.0 V	182.0 V	2.000 V	2.000 V	2.000 V	+	2.021 s

Assess: + .. Passed x .. Failed o .. Not assessed

### Assessment Statistics

Name	Ramp	Condition	Sig	Nom.	Act.Av.	min	max	Std. Dev.	Assess
------	------	-----------	-----	------	---------	-----	-----	-----------	--------

Assess: + .. Passed x .. Failed o .. Not assessed

### Calculation Results

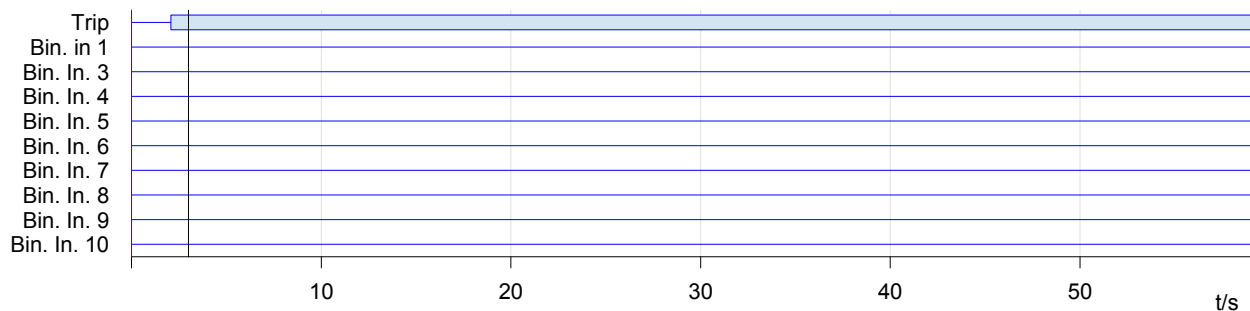
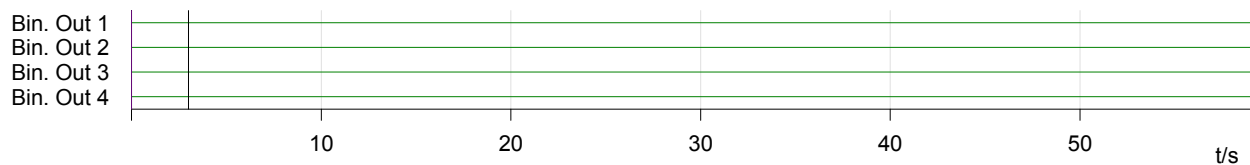
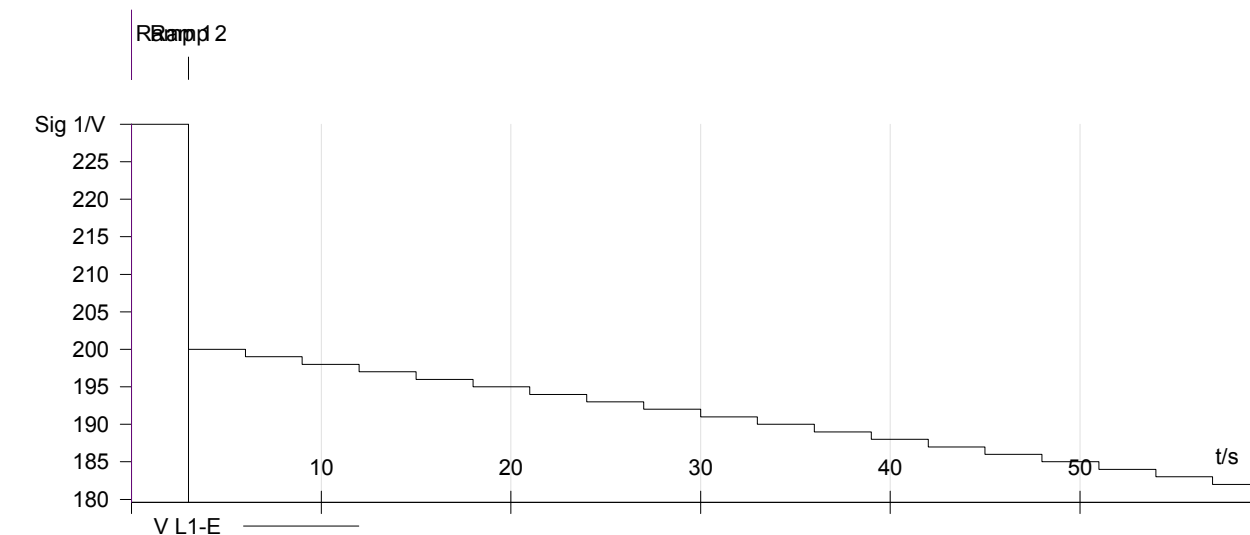
Name/ Exec.	Calc.	X	Y	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess
-------------	-------	---	---	------	------	-------	-------	------	--------

Assess: + .. Passed x .. Failed o .. Not assessed

### Calculation Statistics

Name	Calc.	X	Y	Nom.	Act.Av.	min	max	Std. Dev.	Assess
------	-------	---	---	------	---------	-----	-----	-----------	--------

Assess: + .. Passed x .. Failed o .. Not assessed





## Cursor Data

	Time	Signal	Value
Cursor 1	0.000 s	<none>	n/a
Cursor 2	59.02 s	<none>	n/a
C2 - C1	59.02 s		n/a

## Test State:

Test passed

## Under Voltage L2 (27P):

## Test Settings

### General

No. of ramp states: 2  
 Total steps per test: 27  
 Total time per test: 81.000 s  
 No. of test executions: 1

Input Mode: Direct  
 Fault Type:

### Ramped Quantities

V L2-E / Magnitude

### Ramp States

Ramp	Ramp 1	Ramp 2
V L1-E	230.0 V 0.00 ° 50.000 Hz	230.0 V 0.00 ° 50.000 Hz
V L2-E	230.0 V -120.00 ° 50.000 Hz	200.0 V -120.00 ° 50.000 Hz
V L3-E	230.0 V 120.00 ° 50.000 Hz	230.0 V 120.00 ° 50.000 Hz
Force abs. Phases	Yes	No
Sig 1 From	230.0 V	200.0 V
Sig 1 To	230.0 V	175.0 V
Sig 1 Delta	0.000 V	-1.000 V
Sig 1 d/dt	-1.667 V/s	-333.3 mV/s
Bin. Out 1	0	0
Bin. Out 2	0	0
Bin. Out 3	0	0
Bin. Out 4	0	0
dt per Step	3.000 s	3.000 s
Ramp Steps	1	26
Ramp Time	3.000s	78.000s
Trigger	None	Bin
Trigger Logic		OR
Trip		0
Bin. In 1		X
Bin. In. 3		X
Bin. In. 4		X
Bin. In. 5		X
Bin. In. 6		X
Bin. In. 7		X
Bin. In. 8		X

Bin. In. 9		X
Bin. In. 10		X
Step back	No	No
Delay Time	0.000 s	0.000 s

## Test Module

Name: OMICRON Ramping Version: 3.20  
 Test Start: 01-Dec-2017 10:53:07 Test End: 01-Dec-2017 10:54:11  
 User Name: Dileepa Manager: Shanaka  
 Company: Dara Switchboards

## Test Results

### Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Trip	Ramp 2	Trip 1->0	V L2-E	180.0 V	181.0 V	2.000 V	2.000 V	1.000 V	+	2.026 s

Assess: + .. Passed x .. Failed o .. Not assessed

### Assessment Statistics

Name	Ramp	Condition	Sig	Nom.	Act.Av.	min	max	Std. Dev.	Assess
------	------	-----------	-----	------	---------	-----	-----	-----------	--------

Assess: + .. Passed x .. Failed o .. Not assessed

### Calculation Results

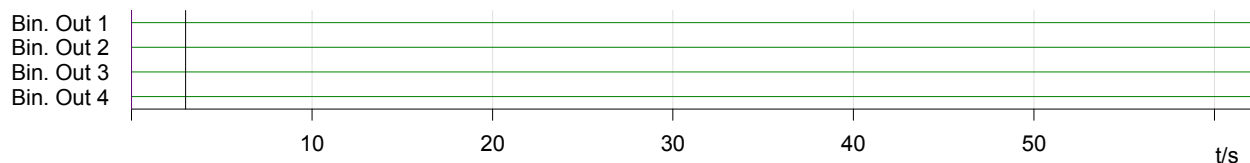
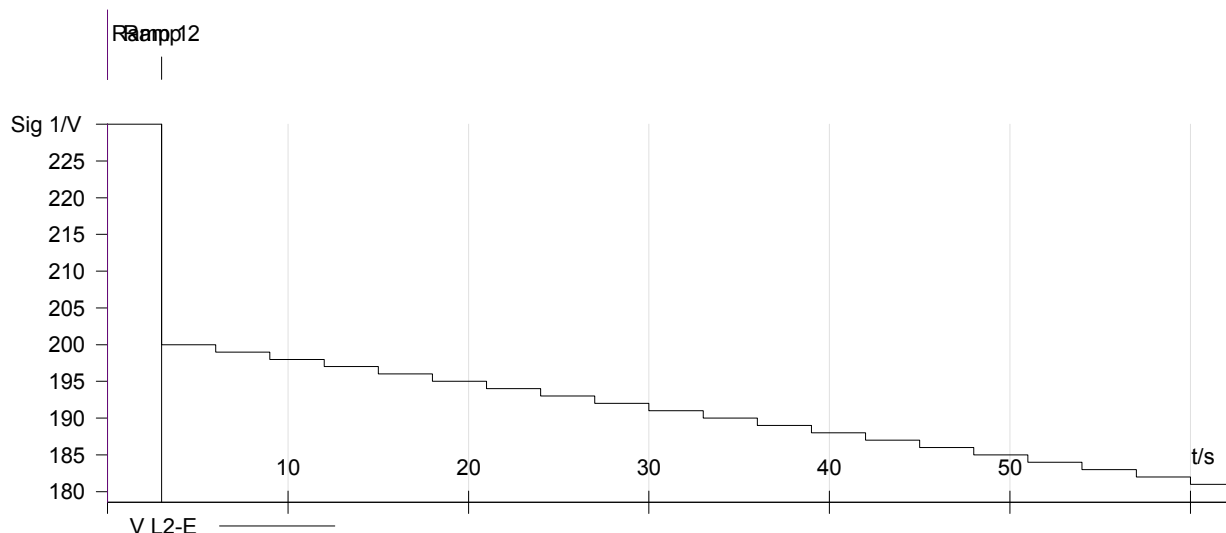
Name/ Exec.	Calc.	X	Y	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess
-------------	-------	---	---	------	------	-------	-------	------	--------

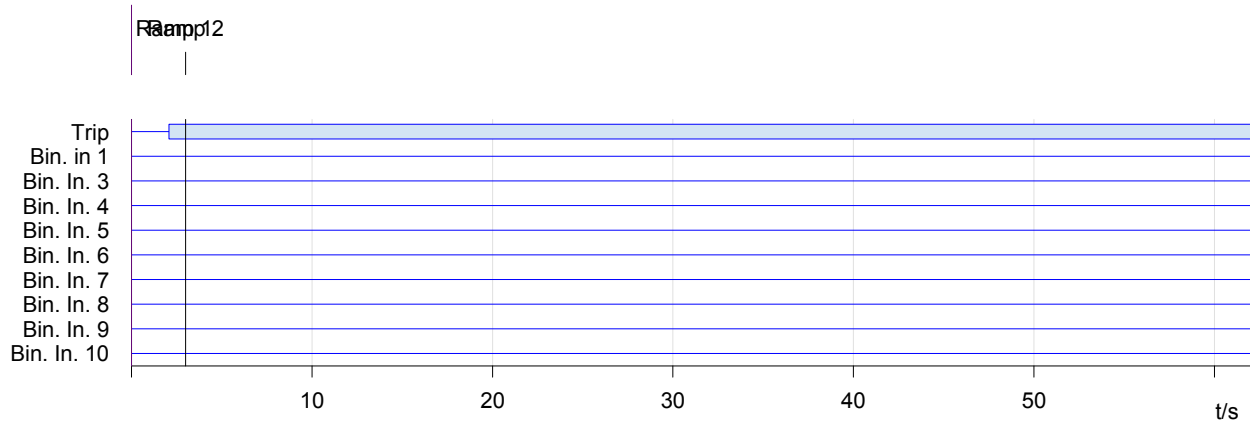
Assess: + .. Passed x .. Failed o .. Not assessed

### Calculation Statistics

Name	Calc.	X	Y	Nom.	Act.Av.	min	max	Std. Dev.	Assess
------	-------	---	---	------	---------	-----	-----	-----------	--------

Assess: + .. Passed x .. Failed o .. Not assessed





### Cursor Data

	Time	Signal	Value
Cursor 1	0.000 s	<none>	n/a
Cursor 2	62.03 s	<none>	n/a
C2 - C1	62.03 s		n/a

### Test State:

Test passed

### Under Voltage L3 (27P):

### Test Settings

#### General

No. of ramp states: 2  
 Total steps per test: 27  
 Total time per test: 81.000 s  
 No. of test executions: 1

Input Mode: Direct  
 Fault Type:

### Ramped Quantities

V L3-E / Magnitude

#### Ramp States

Ramp	Ramp 1	Ramp 2
V L1-E	230.0 V 0.00 ° 50.000 Hz	230.0 V 0.00 ° 50.000 Hz
V L2-E	230.0 V -120.00 ° 50.000 Hz	230.0 V -120.00 ° 50.000 Hz
V L3-E	230.0 V 120.00 ° 50.000 Hz	200.0 V 120.00 ° 50.000 Hz
Force abs. Phases	Yes	No
Sig 1 From	230.0 V	200.0 V
Sig 1 To	230.0 V	175.0 V
Sig 1 Delta	0.000 V	-1.000 V
Sig 1 d/dt	-1.667 V/s	-333.3 mV/s
Bin. Out 1	0	0

Bin. Out 2	0	0
Bin. Out 3	0	0
Bin. Out 4	0	0
dt per Step	3.000 s	3.000 s
Ramp Steps	1	26
Ramp Time	3.000s	78.000s
Trigger	None	Bin
Trigger Logic		OR
Trip		0
Bin. in 1		X
Bin. In. 3		X
Bin. In. 4		X
Bin. In. 5		X
Bin. In. 6		X
Bin. In. 7		X
Bin. In. 8		X
Bin. In. 9		X
Bin. In. 10		X
Step back	No	No
Delay Time	0.000 s	0.000 s

## Test Module

Name: OMICRON Ramping  
 Test Start: 01-Dec-2017 10:54:41  
 User Name: Dileepa  
 Company: Dara Switchboards

Version: 3.20  
 Test End: 01-Dec-2017 10:55:45  
 Manager: Shanaka

## Test Results

### Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Trip	Ramp 2	Trip 1->0	V L3-E	180.0 V	181.0 V	2.000 V	2.000 V	1.000 V	+	2.024 s

Assess: + .. Passed x .. Failed o .. Not assessed

### Assessment Statistics

Name	Ramp	Condition	Sig	Nom.	Act.Av.	min	max	Std. Dev.	Assess
------	------	-----------	-----	------	---------	-----	-----	-----------	--------

Assess: + .. Passed x .. Failed o .. Not assessed

### Calculation Results

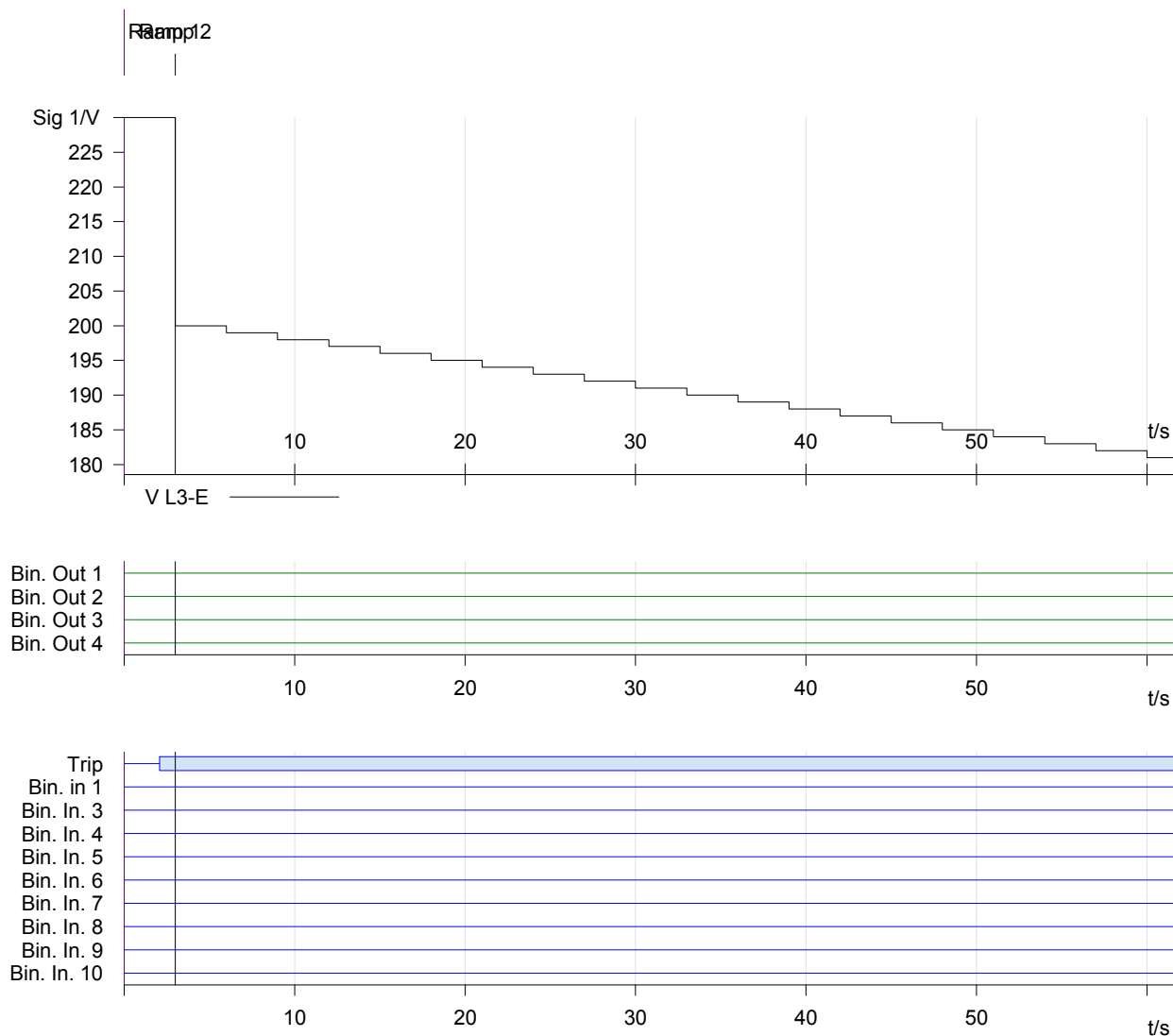
Name/ Exec.	Calc.	X	Y	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess
-------------	-------	---	---	------	------	-------	-------	------	--------

Assess: + .. Passed x .. Failed o .. Not assessed

### Calculation Statistics

Name	Calc.	X	Y	Nom.	Act.Av.	min	max	Std. Dev.	Assess
------	-------	---	---	------	---------	-----	-----	-----------	--------

Assess: + .. Passed x .. Failed o .. Not assessed



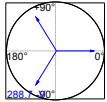

### Cursor Data

	Time	Signal	Value
Cursor 1	0.000 s	<none>	n/a
Cursor 2	62.02 s	<none>	n/a
C2 - C1	62.02 s		n/a

**Test State:**  
**Test passed**

## Under Voltage Time L1 (27P):

### Test Settings

State	State 1	State 2
V L1-E	230.0 V 0.00 ° 50.000 Hz	175.0 V 0.00 ° 50.000 Hz
V L2-E	230.0 V -120.00 ° 50.000 Hz	230.0 V -120.00 ° 50.000 Hz
V L3-E	230.0 V 120.00 ° 50.000 Hz	230.0 V 120.00 ° 50.000 Hz
Bin. Out 1	0	0
Bin. Out 2	0	0
Bin. Out 3	0	0
Bin. Out 4	0	0
Max. State Time	3.000 s	3.000 s
Trigger Logic		OR
Trip		0
User interaction	no	no
CMGPS trigger	no	no
IRIG-B/PTP trigger	no	no
Pulses / seconds	1	1
Delay after Tr.	0.000 s	0.000 s
On trigger jump to test end	no	no
Diagrams		

### Comment

### Test Module

Name:	OMICRON State Sequencer	Version:	3.20
Test Start:	01-Dec-2017 10:56:06	Test End:	01-Dec-2017 10:56:12
User Name:	Dileepa	Manager:	Shanaka
Company:	Dara Switchboards		

### Test Results

#### Time Assessment

Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
U/V Timing	State 2	State 2	Trip 1>0	2.000 s	100.0 ms	100.0 s	2.033 s	32.70 ms	+

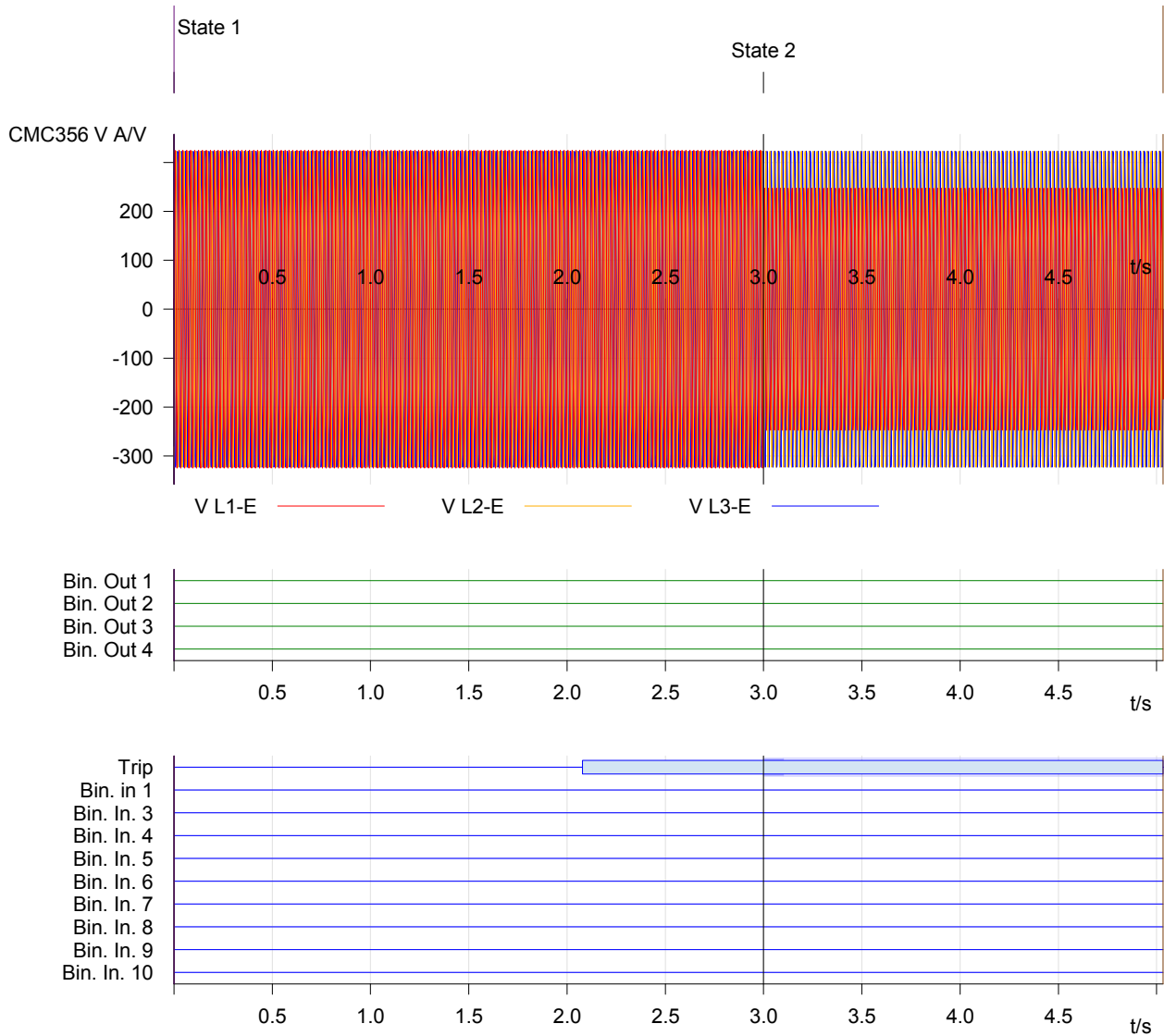
Assess: + .. Passed x .. Failed o .. Not assessed

#### State Assessment

	State 1	State 2
Assess	+	+
Tolerance	0.000 s	100.0 ms

<b>Trip</b>	X	1
-------------	---	---

Assess: + .. Passed x .. Failed o .. Not assessed



#### Cursor Data

	Time	Signal	Value
Cursor 1	0.00 s	<none>	n/a
Cursor 2	5.03 s	<none>	n/a
C2 - C1	5.03 s		n/a

#### Event recorder

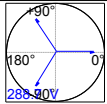
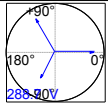
Time	Type	Signal name	Slope
2.079 s	Input	Trip	0>1
5.033 s	Input	Trip	1>0



Test State:  
Test passed

## Under Voltage Time L2 (27P):

### Test Settings

State	State 1	State 2
V L1-E	230.0 V 0.00 ° 50.000 Hz	230.0 V 0.00 ° 50.000 Hz
V L2-E	230.0 V -120.00 ° 50.000 Hz	175.0 V -120.00 ° 50.000 Hz
V L3-E	230.0 V 120.00 ° 50.000 Hz	230.0 V 120.00 ° 50.000 Hz
Bin. Out 1	0	0
Bin. Out 2	0	0
Bin. Out 3	0	0
Bin. Out 4	0	0
Max. State Time	3.000 s	3.000 s
Trigger Logic		OR
Trip		0
User interaction	no	no
CMGPS trigger	no	no
IRIG-B/PTP trigger	no	no
Pulses / seconds	1	1
Delay after Tr.	0.000 s	0.000 s
On trigger jump to test end	no	no
Diagrams		

### Comment

### Test Module

Name:	OMICRON State Sequencer	Version:	3.20
Test Start:	01-Dec-2017 11:02:23	Test End:	01-Dec-2017 11:02:30
User Name:	Dileepa	Manager:	Shanaka
Company:	Dara Switchboards		

### Test Results

#### Time Assessment

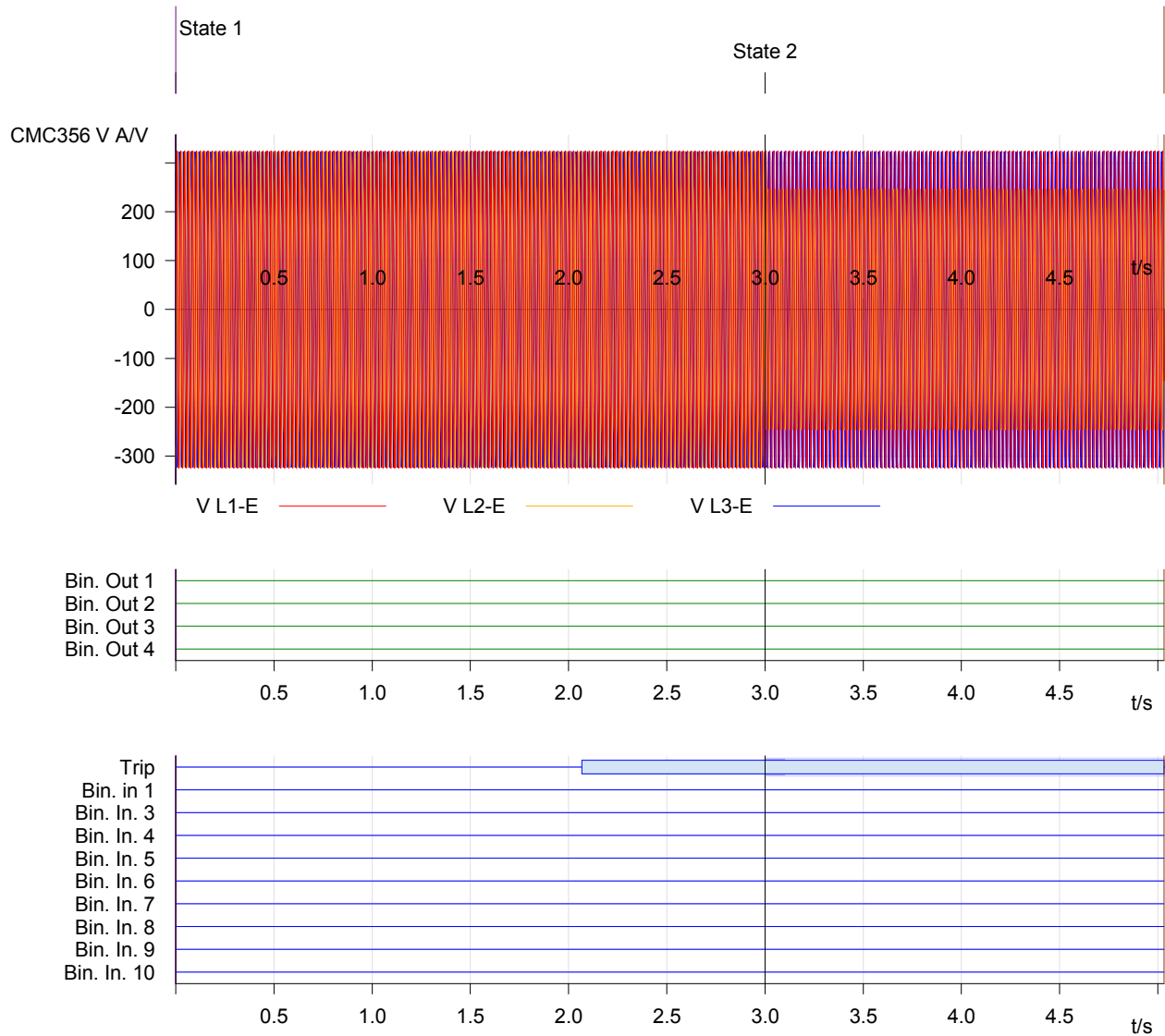
Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
U/V Timing	State 2	State 2	Trip 1>0	2.000 s	100.0 ms	100.0 ms	2.032 s	31.50 ms	+

Assess: + .. Passed x .. Failed o .. Not assessed

## State Assessment

	State 1	State 2
Assess	+	+
Tolerance	0.000 s	100.0 ms
Trip	X	1

Assess: + .. Passed x .. Failed o .. Not assessed



## Cursor Data

	Time	Signal	Value
Cursor 1	0.000 s	<none>	n/a
Cursor 2	5.032 s	<none>	n/a
C2 - C1	5.032 s		n/a

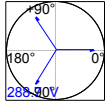
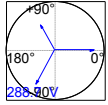
## Event recorder

Time	Type	Signal name	Slope
2.068 s	Input	Trip	0>1
5.032 s	Input	Trip	1>0

Test State:  
Test passed

## Under Voltage Time L3 (27P):

### Test Settings

State	State 1	State 2
V L1-E	230.0 V 0.00 ° 50.000 Hz	230.0 V 0.00 ° 50.000 Hz
V L2-E	230.0 V -120.00 ° 50.000 Hz	230.0 V -120.00 ° 50.000 Hz
V L3-E	230.0 V 120.00 ° 50.000 Hz	175.0 V 120.00 ° 50.000 Hz
Bin. Out 1	0	0
Bin. Out 2	0	0
Bin. Out 3	0	0
Bin. Out 4	0	0
Max. State Time	3.000 s	3.000 s
Trigger Logic		OR
Trip		0
User interaction	no	no
CMGPS trigger	no	no
IRIG-B/PTP trigger	no	no
Pulses / seconds	1	1
Delay after Tr.	0.000 s	0.000 s
On trigger jump to test end	no	no
Diagrams		

### Comment

### Test Module

Name:	OMICRON State Sequencer	Version:	3.20
Test Start:	01-Dec-2017 11:03:32	Test End:	01-Dec-2017 11:03:39
User Name:	Dileepa	Manager:	Shanaka
Company:	Dara Switchboards		

### Test Results

#### Time Assessment

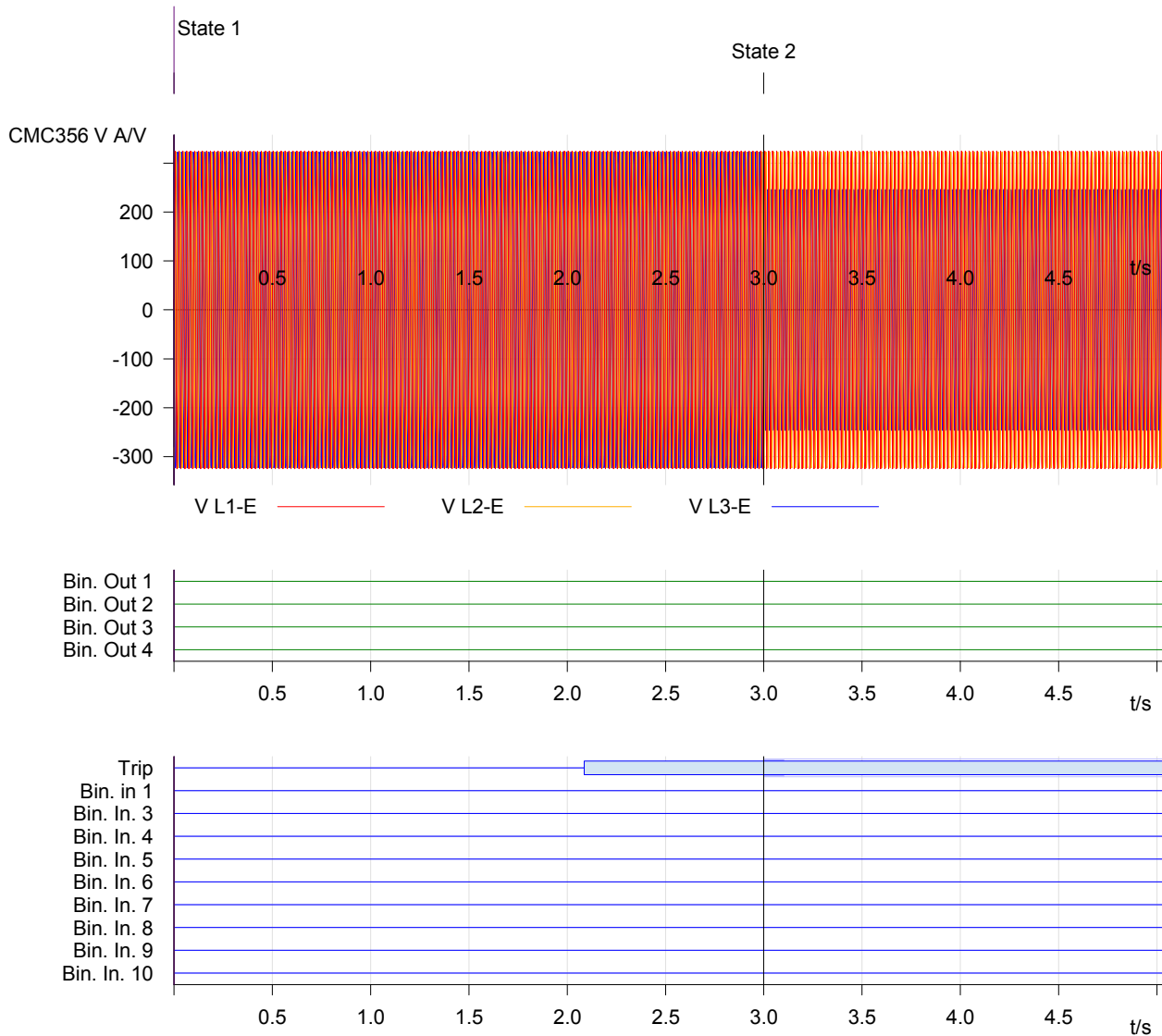
Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
U/V Timing	State 2	State 2	Trip 1>0	2.000 s	100.0 ms	100.0 ms	2.030 s	30.10 ms	+

Assess: + .. Passed x .. Failed o .. Not assessed

#### State Assessment

	State 1	State 2
Assess	+	+
Tolerance	0.000 s	100.0 ms
Trip	X	1

Assess: + .. Passed x .. Failed o .. Not assessed



#### Cursor Data

	Time	Signal	Value
Cursor 1	0.000 s	<none>	n/a
Cursor 2	5.030 s	<none>	n/a
C2 - C1	5.030 s		n/a

#### Event recorder

Time	Type	Signal name	Slope
2.086 s	Input	Trip	0>1
5.030 s	Input	Trip	1>0

Test State:  
Test passed

## Over Voltage L1 (59P):

### Test Settings

#### General

No. of ramp states: 2  
Total steps per test: 22  
Total time per test: 66.000 s  
No. of test executions: 1

Input Mode: Direct  
Fault Type:

#### Ramped Quantities

V L1-E / Magnitude

#### Ramp States

Ramp	Ramp 1	Ramp 2
V L1-E	230.0 V 0.00 ° 50.000 Hz	250.0 V 0.00 ° 50.000 Hz
V L2-E	240.0 V -120.00 ° 50.000 Hz	240.0 V -120.00 ° 50.000 Hz
V L3-E	240.0 V 120.00 ° 50.000 Hz	240.0 V 120.00 ° 50.000 Hz
Force abs. Phases	Yes	No
Sig 1 From	230.0 V	250.0 V
Sig 1 To	230.0 V	270.0 V
Sig 1 Delta	0.000 V	1.000 V
Sig 1 d/dt	-1.667 V/s	333.3 mV/s
Bin. Out 1	0	0
Bin. Out 2	0	0
Bin. Out 3	0	0
Bin. Out 4	0	0
dt per Step	3.000 s	3.000 s
Ramp Steps	1	21
Ramp Time	3.000s	63.000s
Trigger	None	Bin
Trigger Logic		OR
Trip		0
Bin. in 1		X
Bin. In. 3		X
Bin. In. 4		X
Bin. In. 5		X
Bin. In. 6		X
Bin. In. 7		X
Bin. In. 8		X
Bin. In. 9		X
Bin. In. 10		X
Step back	No	No
Delay Time	0.000 s	0.000 s

## Test Module

Name:	OMICRON Ramping	Version:	3.20
Test Start:	01-Dec-2017 11:03:56	Test End:	01-Dec-2017 11:04:39
User Name:	Dileepa	Manager:	Shanaka
Company:	Dara Switchboards		

## Test Results

### Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Trip	Ramp 2	Trip 1->0	V L1-E	260.0 V	262.0 V	2.000 V	2.000 V	2.000 V	+	1.999 s

Assess: + .. Passed x .. Failed o .. Not assessed

### Assessment Statistics

Name	Ramp	Condition	Sig	Nom.	Act.Av.	min	max	Std. Dev.	Assess
------	------	-----------	-----	------	---------	-----	-----	-----------	--------

Assess: + .. Passed x .. Failed o .. Not assessed

### Calculation Results

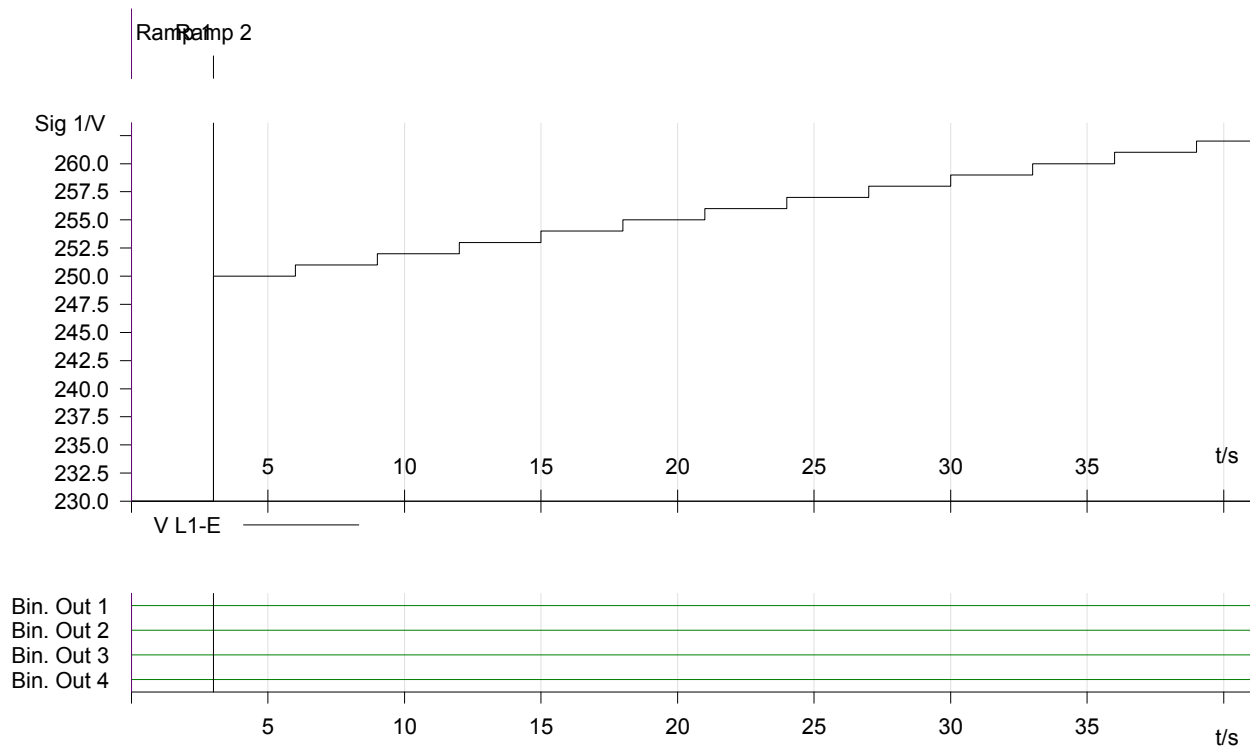
Name/ Exec.	Calc.	X	Y	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess
-------------	-------	---	---	------	------	-------	-------	------	--------

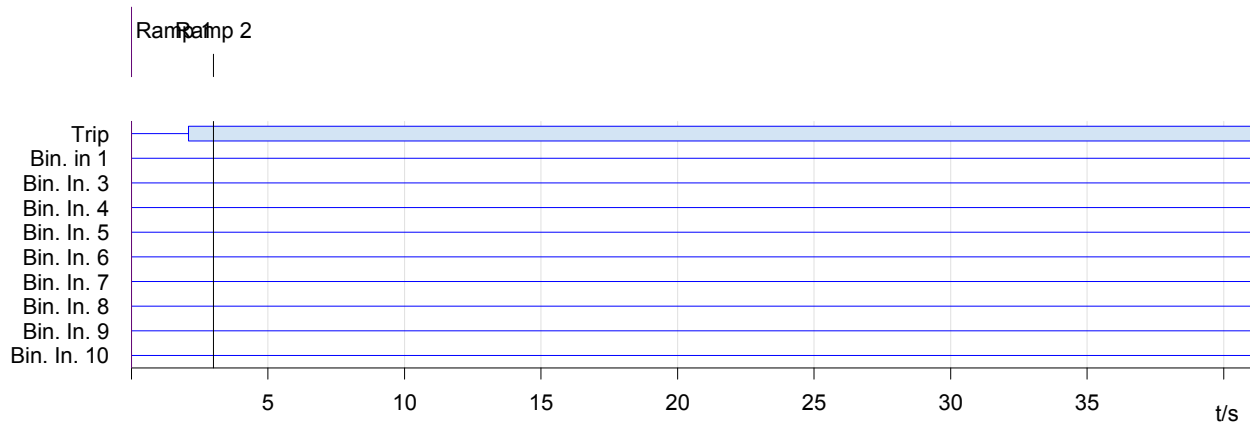
Assess: + .. Passed x .. Failed o .. Not assessed

### Calculation Statistics

Name	Calc.	X	Y	Nom.	Act.Av.	min	max	Std. Dev.	Assess
------	-------	---	---	------	---------	-----	-----	-----------	--------

Assess: + .. Passed x .. Failed o .. Not assessed





### Cursor Data

	Time	Signal	Value
Cursor 1	0.000 s	<none>	n/a
Cursor 2	41.00 s	<none>	n/a
C2 - C1	41.00 s		n/a

### Test State:

Test passed

### Over Voltage L2(59P):

### Test Settings

#### General

No. of ramp states: 2  
Total steps per test: 22  
Total time per test: 66.000 s  
No. of test executions: 1

Input Mode: Direct  
Fault Type:

### Ramped Quantities

V L2-E / Magnitude

#### Ramp States

Ramp	Ramp 1	Ramp 2
V L1-E	230.0 V 0.00 ° 50.000 Hz	230.0 V 0.00 ° 50.000 Hz
V L2-E	230.0 V -120.00 ° 50.000 Hz	250.0 V -120.00 ° 50.000 Hz
V L3-E	230.0 V 120.00 ° 50.000 Hz	230.0 V 120.00 ° 50.000 Hz
Force abs. Phases	Yes	No
Sig 1 From	230.0 V	250.0 V
Sig 1 To	230.0 V	270.0 V
Sig 1 Delta	0.000 V	1.000 V
Sig 1 d/dt	-1.667 V/s	333.3 mV/s
Bin. Out 1	0	0



Bin. Out 2	0	0
Bin. Out 3	0	0
Bin. Out 4	0	0
dt per Step	3.000 s	3.000 s
Ramp Steps	1	21
Ramp Time	3.000s	63.000s
Trigger	None	Bin
Trigger Logic		OR
Trip		0
Bin. in 1		X
Bin. In. 3		X
Bin. In. 4		X
Bin. In. 5		X
Bin. In. 6		X
Bin. In. 7		X
Bin. In. 8		X
Bin. In. 9		X
Bin. In. 10		X
Step back	No	No
Delay Time	0.000 s	0.000 s

## Test Module

Name: OMICRON Ramping  
 Test Start: 01-Dec-2017 11:05:29  
 User Name: Dileepa  
 Company: Dara Switchboards

Version: 3.20  
 Test End: 01-Dec-2017 11:06:09  
 Manager: Shanaka

## Test Results

### Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Trip	Ramp 2	Trip 1->0	V L2-E	260.0 V	261.0 V	2.000 V	2.000 V	1.000 V	+	2.026 s

Assess: + .. Passed x .. Failed o .. Not assessed

### Assessment Statistics

Name	Ramp	Condition	Sig	Nom.	Act.Av.	min	max	Std. Dev.	Assess
------	------	-----------	-----	------	---------	-----	-----	-----------	--------

Assess: + .. Passed x .. Failed o .. Not assessed

### Calculation Results

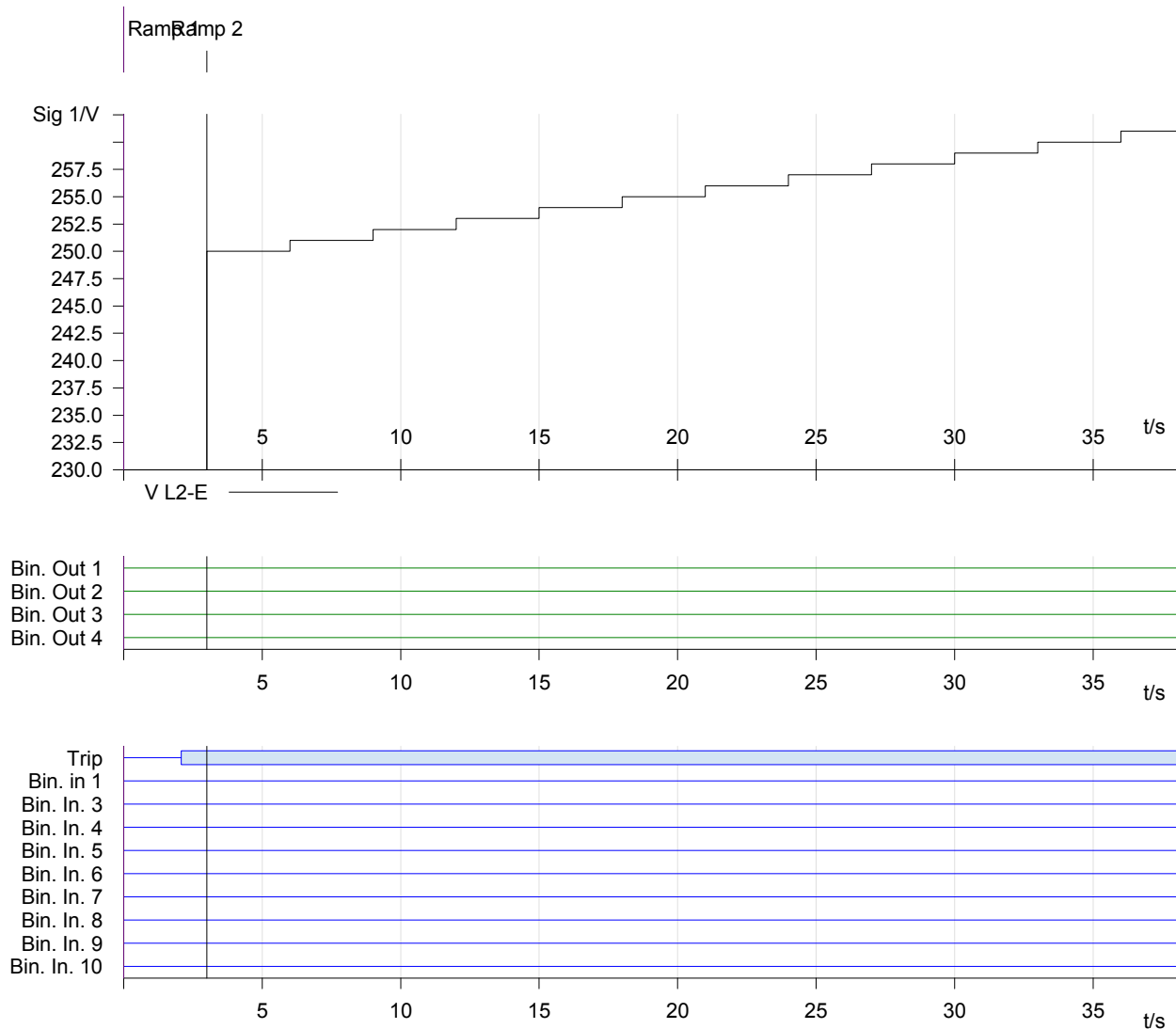
Name/ Exec.	Calc.	X	Y	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess
-------------	-------	---	---	------	------	-------	-------	------	--------

Assess: + .. Passed x .. Failed o .. Not assessed

### Calculation Statistics

Name	Calc.	X	Y	Nom.	Act.Av.	min	max	Std. Dev.	Assess
------	-------	---	---	------	---------	-----	-----	-----------	--------

Assess: + .. Passed x .. Failed o .. Not assessed



#### Cursor Data

	Time	Signal	Value
Cursor 1	0.000 s	<none>	n/a
Cursor 2	38.03 s	<none>	n/a
C2 - C1	38.03 s		n/a

**Test State:**  
**Test passed**

### Over Voltage L3 (59P):

#### Test Settings

##### General

No. of ramp states: 2  
Total steps per test: 22  
Total time per test: 66.000 s  
No. of test executions: 1

Input Mode: Direct  
Fault Type:

## Ramped Quantities

V L3-E / Magnitude

### Ramp States

Ramp	Ramp 1	Ramp 2
V L1-E	230.0 V 0.00 ° 50.000 Hz	230.0 V 0.00 ° 50.000 Hz
V L2-E	230.0 V -120.00 ° 50.000 Hz	230.0 V -120.00 ° 50.000 Hz
V L3-E	230.0 V 120.00 ° 50.000 Hz	250.0 V 120.00 ° 50.000 Hz
Force abs. Phases	Yes	No
Sig 1 From	230.0 V	250.0 V
Sig 1 To	230.0 V	270.0 V
Sig 1 Delta	0.000 V	1.000 V
Sig 1 d/dt	-1.667 V/s	333.3 mV/s
Bin. Out 1	0	0
Bin. Out 2	0	0
Bin. Out 3	0	0
Bin. Out 4	0	0
dt per Step	3.000 s	3.000 s
Ramp Steps	1	21
Ramp Time	3.000s	63.000s
Trigger	None	Bin
Trigger Logic		OR
Trip		0
Bin. in 1		X
Bin. In. 3		X
Bin. In. 4		X
Bin. In. 5		X
Bin. In. 6		X
Bin. In. 7		X
Bin. In. 8		X
Bin. In. 9		X
Bin. In. 10		X
Step back	No	No
Delay Time	0.000 s	0.000 s

## Test Module

Name: OMICRON Ramping  
Test Start: 01-Dec-2017 11:06:52  
User Name: Dileepa  
Company: Dara Switchboards

Version: 3.20  
Test End: 01-Dec-2017 11:07:35  
Manager: Shanaka

## Test Results

### Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
Trip	Ramp 2	Trip 1->0	V L3-E	260.0 V	262.0 V	2.000 V	2.000 V	2.000 V	+	2.020 s

Assess: + .. Passed x .. Failed o .. Not assessed

### Assessment

## Statistics

Name	Ramp	Condition	Sig	Nom.	Act.Av.	min	max	Std. Dev.	Assess
------	------	-----------	-----	------	---------	-----	-----	-----------	--------

Assess: + .. Passed x .. Failed o .. Not assessed

## Calculation Results

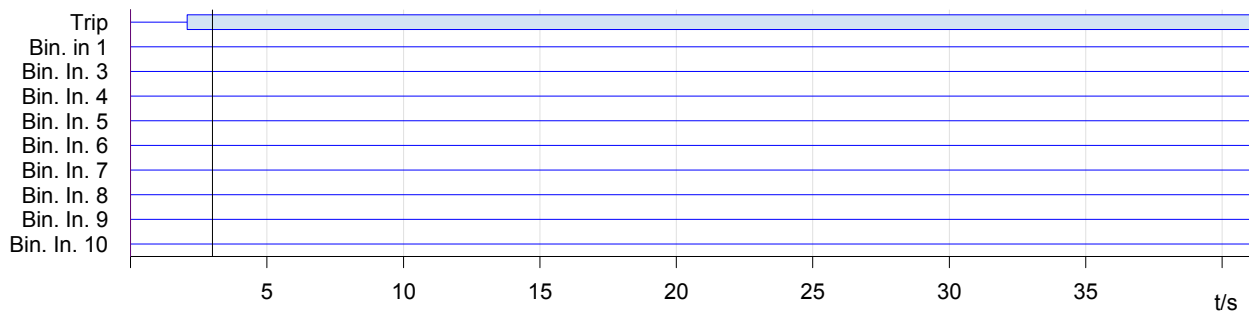
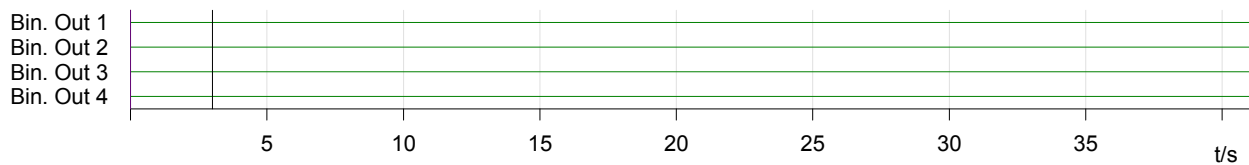
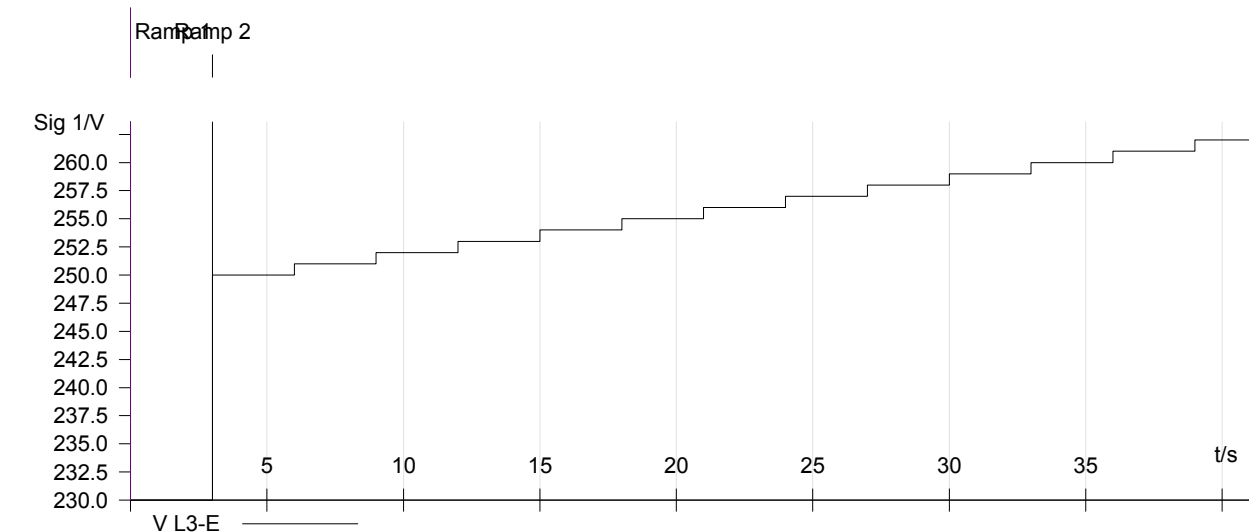
Name/ Exec.	Calc.	X	Y	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess
-------------	-------	---	---	------	------	-------	-------	------	--------

Assess: + .. Passed x .. Failed o .. Not assessed

## Calculation Statistics

Name	Calc.	X	Y	Nom.	Act.Av.	min	max	Std. Dev.	Assess
------	-------	---	---	------	---------	-----	-----	-----------	--------

Assess: + .. Passed x .. Failed o .. Not assessed



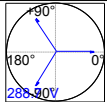
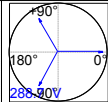
## Cursor Data

	Time	Signal	Value
Cursor 1	0.000 s	<none>	n/a
Cursor 2	41.02 s	<none>	n/a
C2 - C1	41.02 s		n/a

Test State:  
Test passed

## Over Voltage Time L1 (59P):

### Test Settings

State	State 1	State 2
V L1-E	230.0 V 0.00 ° 50.000 Hz	265.0 V 0.00 ° 50.000 Hz
V L2-E	230.0 V -120.00 ° 50.000 Hz	230.0 V -120.00 ° 50.000 Hz
V L3-E	230.0 V 120.00 ° 50.000 Hz	230.0 V 120.00 ° 50.000 Hz
Bin. Out 1	0	0
Bin. Out 2	0	0
Bin. Out 3	0	0
Bin. Out 4	0	0
Max. State Time	3.000 s	3.000 s
Trigger Logic		OR
Trip		0
User interaction	no	no
CMGPS trigger	no	no
IRIG-B/PTP trigger	no	no
Pulses / seconds	1	1
Delay after Tr.	0.000 s	0.000 s
On trigger jump to test end	no	no
Diagrams		

### Comment

### Test Module

Name:	OMICRON State Sequencer	Version:	3.20
Test Start:	01-Dec-2017 11:08:11	Test End:	01-Dec-2017 11:08:18
User Name:	Dileepa	Manager:	Shanaka
Company:	Dara Switchboards		

### Test Results

#### Time Assessment

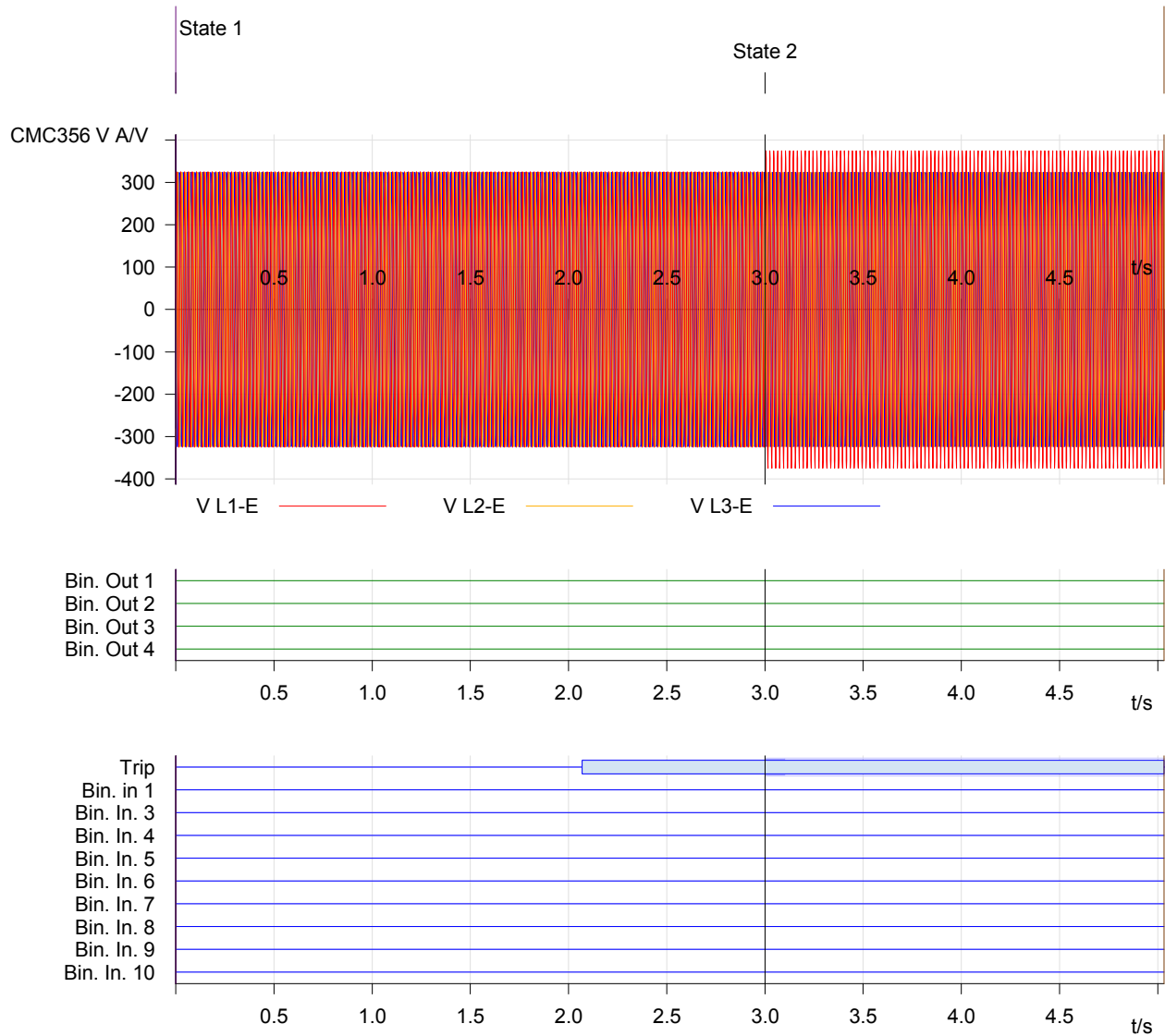
Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
O/V Timing	State 2	State 2	Trip 1>0	2.000 s	100.0 ms	100.0 s	2.032 s	32.20 ms	+

Assess: + .. Passed x .. Failed o .. Not assessed

## State Assessment

	State 1	State 2
Assess	+	+
Tolerance	0.000 s	100.0 ms
Trip	X	1

Assess: + .. Passed x .. Failed o .. Not assessed



## Cursor Data

	Time	Signal	Value
Cursor 1	0.000 s	<none>	n/a
Cursor 2	5.032 s	<none>	n/a
C2 - C1	5.032 s		n/a

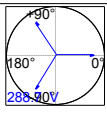
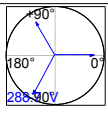
## Event recorder

Time	Type	Signal name	Slope
2.069 s	Input	Trip	0>1
5.032 s	Input	Trip	1>0

Test State:  
Test passed

## Over Voltage Time L2 (59P):

### Test Settings

State	State 1	State 2
V L1-E	230.0 V 0.00 ° 50.000 Hz	230.0 V 0.00 ° 50.000 Hz
V L2-E	230.0 V -120.00 ° 50.000 Hz	265.0 V -120.00 ° 50.000 Hz
V L3-E	230.0 V 120.00 ° 50.000 Hz	230.0 V 120.00 ° 50.000 Hz
Bin. Out 1	0	0
Bin. Out 2	0	0
Bin. Out 3	0	0
Bin. Out 4	0	0
Max. State Time	3.000 s	3.000 s
Trigger Logic		OR
Trip		0
User interaction	no	no
CMGPS trigger	no	no
IRIG-B/PTP trigger	no	no
Pulses / seconds	1	1
Delay after Tr.	0.000 s	0.000 s
On trigger jump to test end	no	no
Diagrams		

### Comment

### Test Module

Name:	OMICRON State Sequencer	Version:	3.20
Test Start:	01-Dec-2017 11:08:44	Test End:	01-Dec-2017 11:08:51
User Name:	Dileepa	Manager:	Shanaka
Company:	Dara Switchboards		

### Test Results

#### Time Assessment

Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
O/V Timing	State 2	State 2	Trip 1>0	2.000 s	100.0 ms	100.0 s	2.034 s	33.80 ms	+

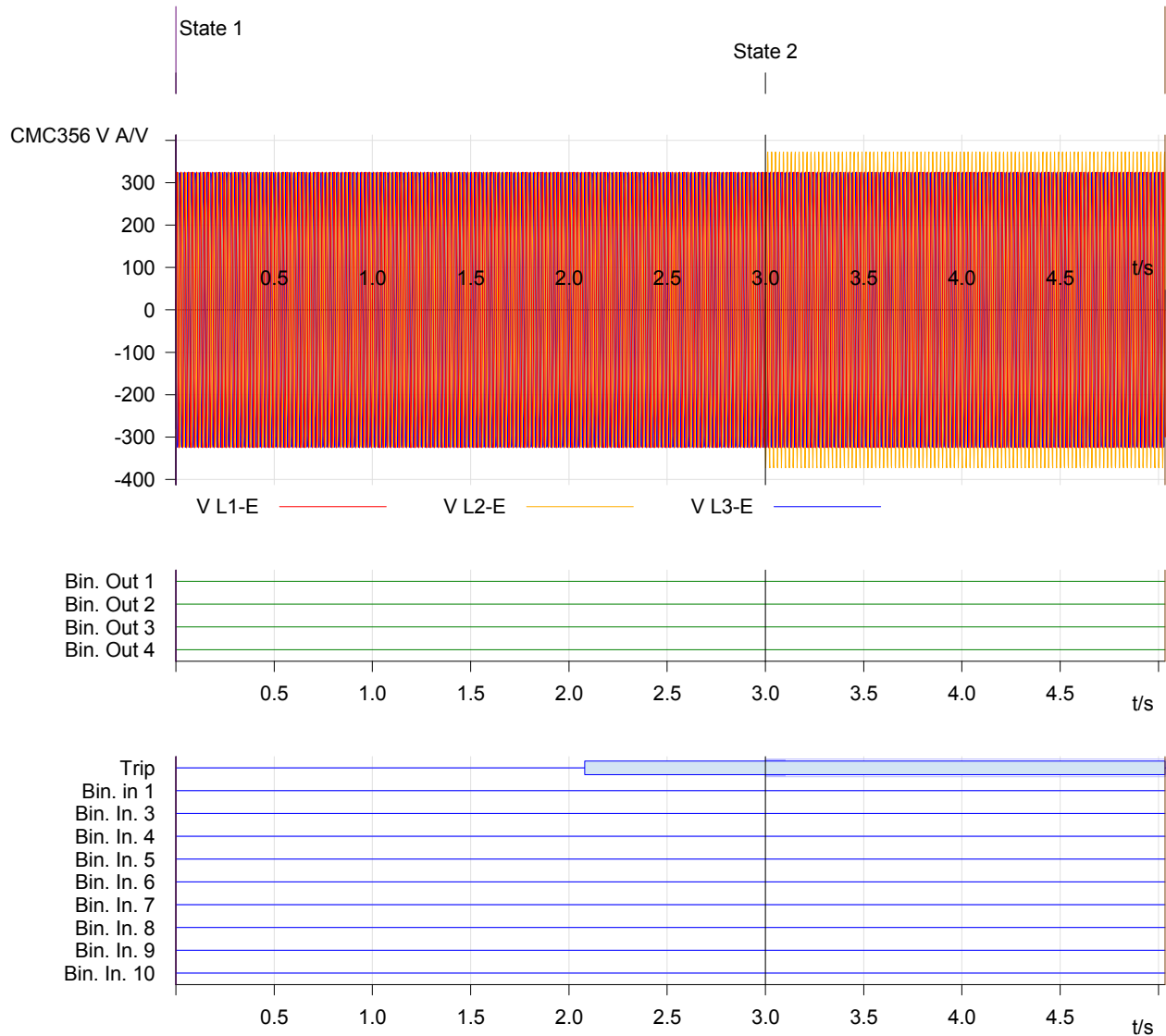
Assess: + .. Passed x .. Failed o .. Not assessed

#### State Assessment



	State 1	State 2
Assess	+	+
Tolerance	0.000 s	100.0 ms
Trip	X	1

Assess: + .. Passed x .. Failed o .. Not assessed



#### Cursor Data

	Time	Signal	Value
Cursor 1	0.000 s	<none>	n/a
Cursor 2	5.034 s	<none>	n/a
C2 - C1	5.034 s		n/a

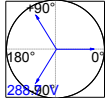
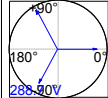
#### Event recorder

Time	Type	Signal name	Slope
2.080 s	Input	Trip	0>1
5.034 s	Input	Trip	1>0

Test State:  
Test passed

## Over Voltage Time L3 (59P):

### Test Settings

State	State 1	State 2
V L1-E	230.0 V 0.00 ° 50.000 Hz	230.0 V 0.00 ° 50.000 Hz
V L2-E	230.0 V -120.00 ° 50.000 Hz	230.0 V -120.00 ° 50.000 Hz
V L3-E	230.0 V 120.00 ° 50.000 Hz	265.0 V 120.00 ° 50.000 Hz
Bin. Out 1	0	0
Bin. Out 2	0	0
Bin. Out 3	0	0
Bin. Out 4	0	0
Max. State Time	3.000 s	3.000 s
Trigger Logic		OR
Trip		0
User interaction	no	no
CMGPS trigger	no	no
IRIG-B/PTP trigger	no	no
Pulses / seconds	1	1
Delay after Tr.	0.000 s	0.000 s
On trigger jump to test end	no	no
Diagrams		

### Comment

### Test Module

Name:	OMICRON State Sequencer	Version:	3.20
Test Start:	01-Dec-2017 11:09:20	Test End:	01-Dec-2017 11:09:27
User Name:	Dileepa	Manager:	Shanaka
Company:	Dara Switchboards		

### Test Results

#### Time Assessment

Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
O/V Timing	State 2	State 2	Trip 1>0	2.000 s	100.0 ms	100.0 s	2.032 s	32.10 ms	+

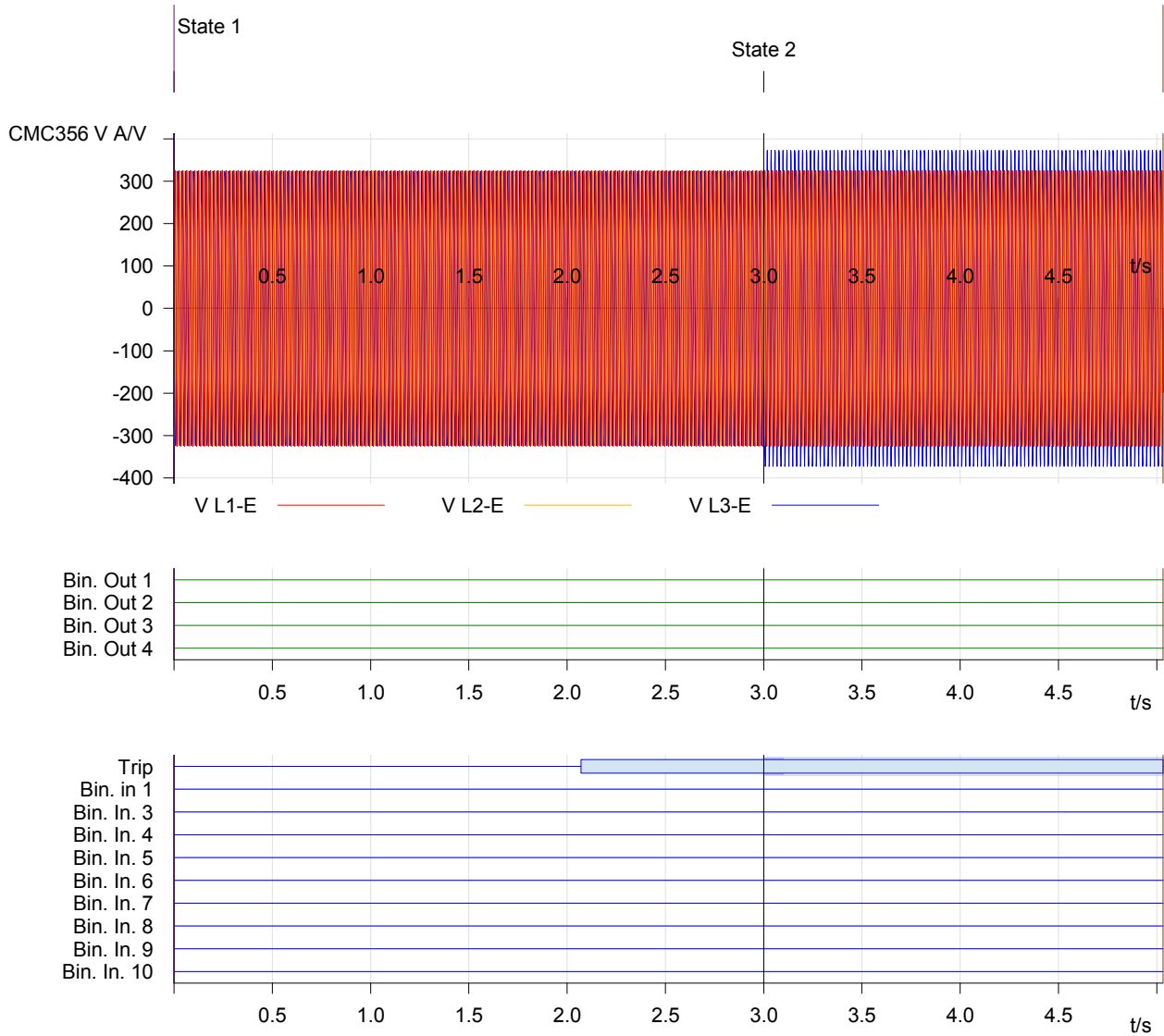
Assess: + .. Passed x .. Failed o .. Not assessed

#### State Assessment

	State 1	State 2
--	---------	---------

Assess	+	+
Tolerance	0.000 s	100.0 ms
Trip	X	1

Assess: + .. Passed x .. Failed o .. Not assessed



### Cursor Data

	Time	Signal	Value
Cursor 1	0.000 s	<none>	n/a
Cursor 2	5.032 s	<none>	n/a
C2 - C1	5.032 s		n/a

### Event recorder

Time	Type	Signal name	Slope
2.070 s	Input	Trip	0>1
5.032 s	Input	Trip	1>0

Test State:

Test passed

## Under Frequency (81U):

### Test Settings

#### General

No. of ramp states: 2  
 Total steps per test: 52  
 Total time per test: 156.000 s  
 No. of test executions: 1

Input Mode: Direct  
 Fault Type:

#### Ramped Quantities

V L1-E, L2-E, L3-E / Frequency

#### Ramp States

Ramp	Ramp 1	Ramp 2
V L1-E	230.0 V 0.00 ° 50.000 Hz	240.0 V 0.00 ° 50.000 Hz
V L2-E	230.0 V -120.00 ° 50.000 Hz	240.0 V -120.00 ° 50.000 Hz
V L3-E	230.0 V 120.00 ° 50.000 Hz	240.0 V 120.00 ° 50.000 Hz
Force abs. Phases	Yes	No
Sig 1 From	50.000 Hz	50.000 Hz
Sig 1 To	50.000 Hz	45.000 Hz
Sig 1 Delta	0.0000 Hz	-100.00 mHz
Sig 1 d/dt	16.67 mHz/s	-33.33 mHz/s
Bin. Out 1	0	0
Bin. Out 2	0	0
Bin. Out 3	0	0
Bin. Out 4	0	0
dt per Step	3.000 s	3.000 s
Ramp Steps	1	51
Ramp Time	3.000s	153.000s
Trigger	None	Bin
Trigger Logic		OR
Trip		0
Bin. in 1		X
Bin. In. 3		X
Bin. In. 4		X
Bin. In. 5		X
Bin. In. 6		X
Bin. In. 7		X
Bin. In. 8		X
Bin. In. 9		X
Bin. In. 10		X
Step back	No	No
Delay Time	0.000 s	0.000 s

## Test Module

Name:	OMICRON Ramping	Version:	3.20
Test Start:	01-Dec-2017 11:09:44	Test End:	01-Dec-2017 11:11:09
User Name:	Dileepa	Manager:	Shanaka
Company:	Dara Switchboards		

## Test Results

### Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
U/Freq.	Ramp 2	Trip 1->0	V L1-E, L2-E, L3-E	47.500 Hz	47.400 Hz	100.00 mHz	100.00 mHz	-100.00 mHz	+	1.876 s

Assess: + .. Passed x .. Failed o .. Not assessed

### Assessment Statistics

Name	Ramp	Condition	Sig	Nom.	Act.Av.	min	max	Std. Dev.	Assess
------	------	-----------	-----	------	---------	-----	-----	-----------	--------

Assess: + .. Passed x .. Failed o .. Not assessed

### Calculation Results

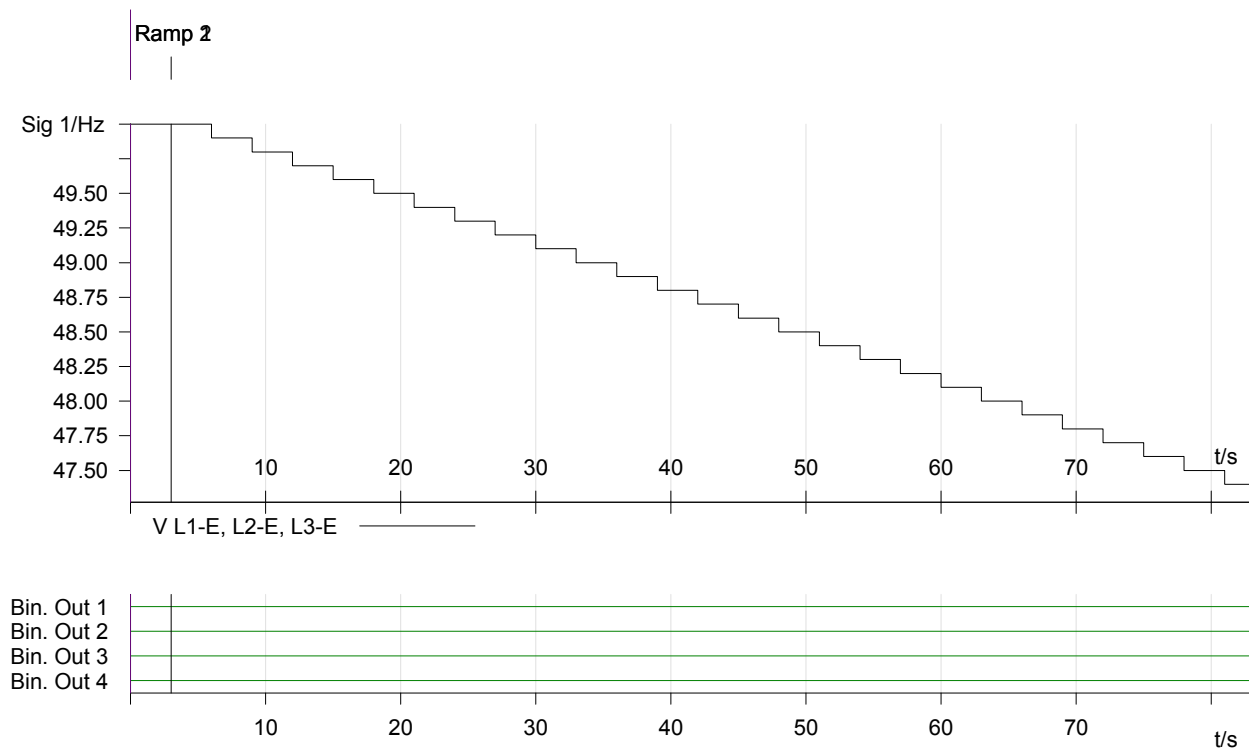
Name/ Exec.	Calc.	X	Y	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess
-------------	-------	---	---	------	------	-------	-------	------	--------

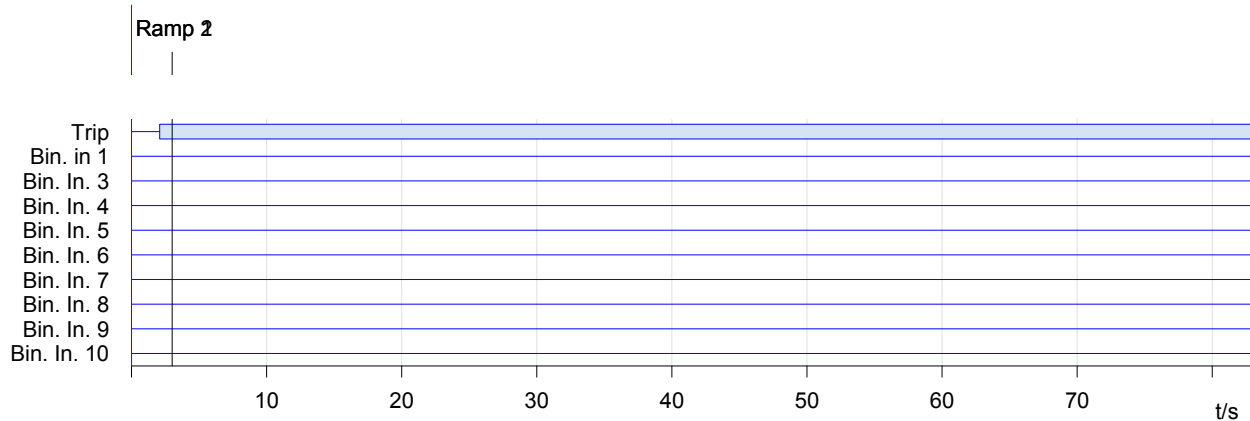
Assess: + .. Passed x .. Failed o .. Not assessed

### Calculation Statistics

Name	Calc.	X	Y	Nom.	Act.Av.	min	max	Std. Dev.	Assess
------	-------	---	---	------	---------	-----	-----	-----------	--------

Assess: + .. Passed x .. Failed o .. Not assessed





### Cursor Data

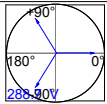
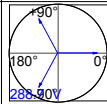
	Time	Signal	Value
Cursor 1	0.000 s	<none>	n/a
Cursor 2	82.88 s	<none>	n/a
C2 - C1	82.88 s		n/a

### Test State:

Test passed

### Under Frequency Time (81U):

### Test Settings

State	State 1	State 2
V L1-E	230.0 V 0.00 ° 50.000 Hz	230.0 V 0.00 ° 45.000 Hz
V L2-E	230.0 V -120.00 ° 50.000 Hz	230.0 V -120.00 ° 45.000 Hz
V L3-E	230.0 V 120.00 ° 50.000 Hz	230.0 V 120.00 ° 45.000 Hz
Bin. Out 1	0	0
Bin. Out 2	0	0
Bin. Out 3	0	0
Bin. Out 4	0	0
Max. State Time	3.000 s	
Trigger Logic		OR
Trip		0
User interaction	no	no
CMGPS trigger	no	no
IRIG-B/PTP trigger	no	no
Pulses / seconds	1	1
Delay after Tr.	0.000 s	0.000 s
On trigger jump to test end	no	no
Diagrams		

## Comment

## Test Module

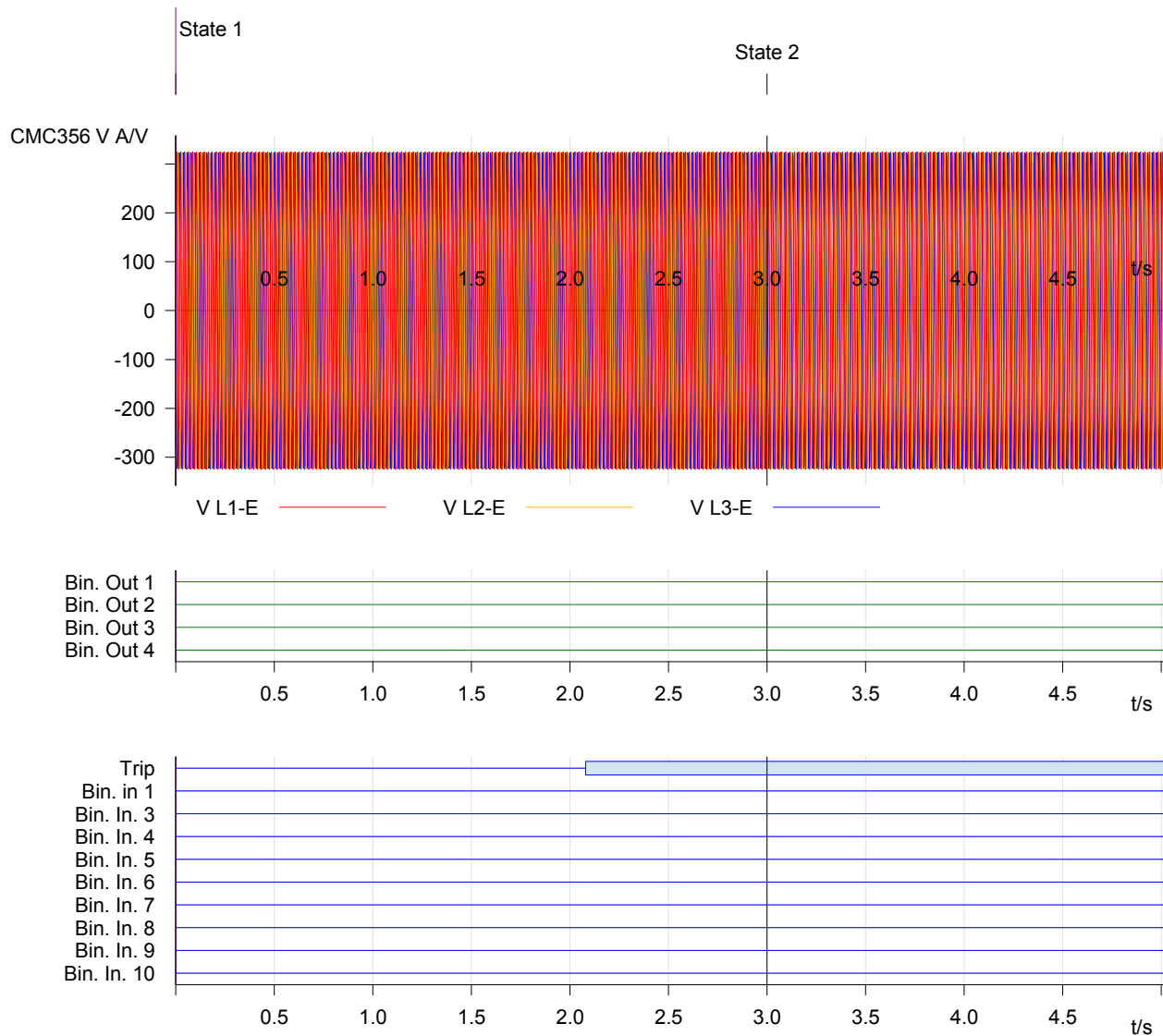
Name:	OMICRON State Sequencer	Version:	3.20
Test Start:	01-Dec-2017 11:11:34	Test End:	01-Dec-2017 11:11:41
User Name:	Dileepa	Manager:	Shanaka
Company:	Dara Switchboards		

## Test Results

### Time Assessment

Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
U/F Time	State 2	State 2	Trip 1>0	2.000 s	100.0 ms	100.0 ms	2.013 s	13.20 ms	+

Assess: + .. Passed x .. Failed o .. Not assessed



## Cursor Data

	Time	Signal	Value
Cursor 1	0.000 s	<none>	n/a
Cursor 2	5.013 s	<none>	n/a
C2 - C1	5.013 s		n/a

#### Event recorder

Time	Type	Signal name	Slope
2.080 s	Input	Trip	0>1
5.013 s	Input	Trip	1>0

#### Test State:

Test passed

### Over Frequency (810):

#### Test Settings

##### General

No. of ramp states: 2  
 Total steps per test: 52  
 Total time per test: 156.000 s  
 No. of test executions: 1

Input Mode: Direct  
 Fault Type:

#### Ramped Quantities

V L1-E, L2-E, L3-E / Frequency

#### Ramp States

Ramp	Ramp 1	Ramp 2
V L1-E	230.0 V 0.00 ° 50.000 Hz	240.0 V 0.00 ° 50.000 Hz
V L2-E	230.0 V -120.00 ° 50.000 Hz	240.0 V -120.00 ° 50.000 Hz
V L3-E	230.0 V 120.00 ° 50.000 Hz	240.0 V 120.00 ° 50.000 Hz
Force abs. Phases	Yes	No
Sig 1 From	50.000 Hz	50.000 Hz
Sig 1 To	50.000 Hz	55.000 Hz
Sig 1 Delta	0.0000 Hz	100.00 mHz
Sig 1 d/dt	16.67 mHz/s	33.33 mHz/s
Bin. Out 1	0	0
Bin. Out 2	0	0
Bin. Out 3	0	0
Bin. Out 4	0	0
dt per Step	3.000 s	3.000 s
Ramp Steps	1	51
Ramp Time	3.000s	153.000s
Trigger	None	Bin
Trigger Logic		OR
Trip		0
Bin. in 1		X
Bin. In. 3		X
Bin. In. 4		X



Bin. In. 5		X
Bin. In. 6		X
Bin. In. 7		X
Bin. In. 8		X
Bin. In. 9		X
Bin. In. 10		X
Step back	No	No
Delay Time	0.000 s	0.000 s

## Test Module

Name: OMICRON Ramping  
 Test Start: 01-Dec-2017 11:12:06  
 User Name: Dileepa  
 Company: Dara Switchboards

Version: 3.20  
 Test End: 01-Dec-2017 11:13:13  
 Manager: Shanaka

## Test Results

### Assessment Results

Name/ Exec.	Ramp	Condition	Sig	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess	Tact
U/Freq.	Ramp 2	Trip 1->0	V L1-E, L2-E, L3-E	52.000 Hz	52.000 Hz	100.00 mHz	100.00 mHz	0.0000 Hz	+	2.037 s

Assess: + .. Passed x .. Failed o .. Not assessed

### Assessment Statistics

Name	Ramp	Condition	Sig	Nom.	Act.Av.	min	max	Std. Dev.	Assess
------	------	-----------	-----	------	---------	-----	-----	-----------	--------

Assess: + .. Passed x .. Failed o .. Not assessed

### Calculation Results

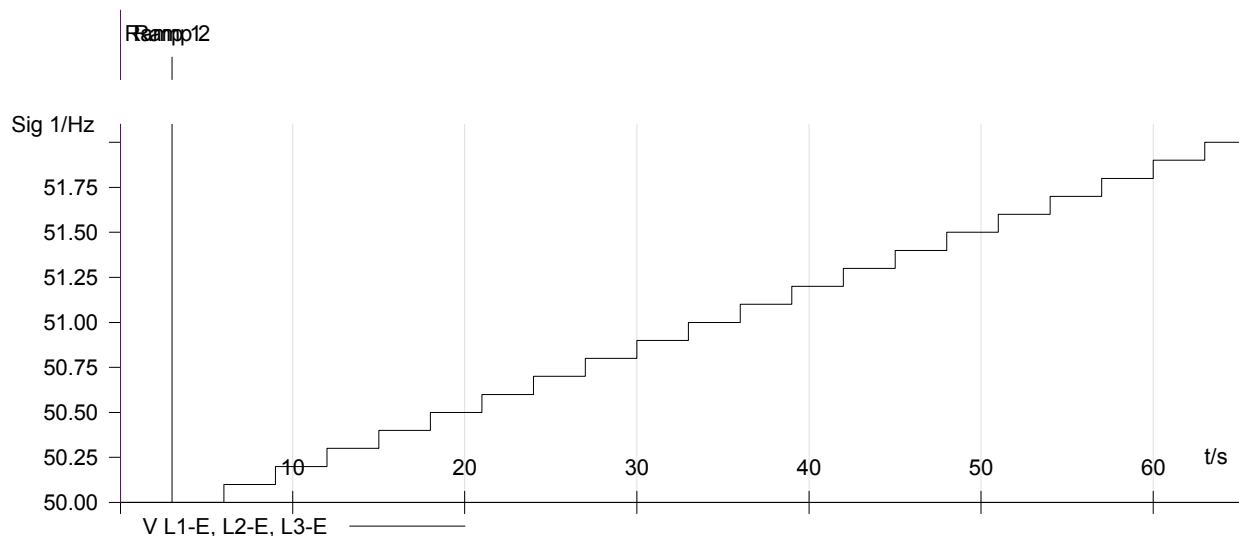
Name/ Exec.	Calc.	X	Y	Nom.	Act.	Tol.-	Tol.+	Dev.	Assess
-------------	-------	---	---	------	------	-------	-------	------	--------

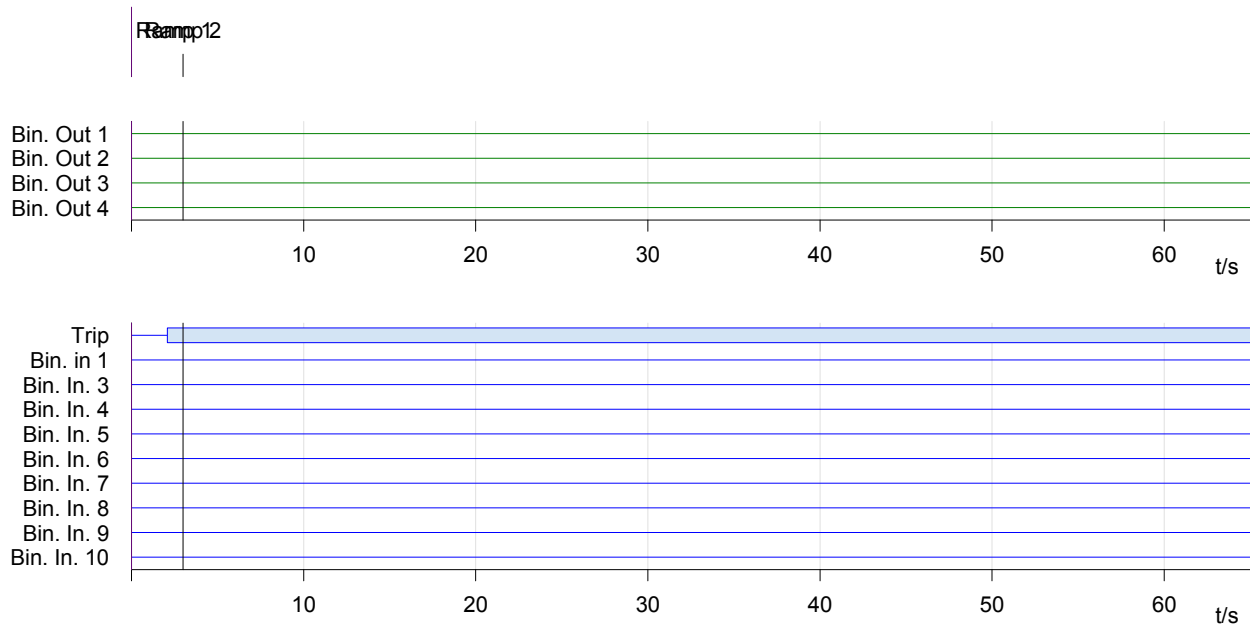
Assess: + .. Passed x .. Failed o .. Not assessed

### Calculation Statistics

Name	Calc.	X	Y	Nom.	Act.Av.	min	max	Std. Dev.	Assess
------	-------	---	---	------	---------	-----	-----	-----------	--------

Assess: + .. Passed x .. Failed o .. Not assessed





#### Cursor Data

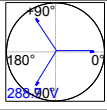
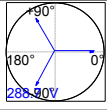
	Time	Signal	Value
Cursor 1	0.000 s	<none>	n/a
Cursor 2	65.04 s	<none>	n/a
C2 - C1	65.04 s		n/a

Test State:  
Test passed

## Over Frequency Time (81O):

#### Test Settings

State	State 1	State 2
V L1-E	230.0 V 0.00 ° 50.000 Hz	230.0 V 0.00 ° 55.000 Hz
V L2-E	230.0 V -120.00 ° 50.000 Hz	230.0 V -120.00 ° 55.000 Hz
V L3-E	230.0 V 120.00 ° 50.000 Hz	230.0 V 120.00 ° 55.000 Hz
Bin. Out 1	0	0
Bin. Out 2	0	0
Bin. Out 3	0	0
Bin. Out 4	0	0
Max. State Time	3.000 s	
Trigger Logic		OR
Trip		0
User interaction	no	no
CMGPS trigger	no	no

IRIG-B/PTP trigger	no	no
Pulses / seconds	1	1
Delay after Tr.	0.000 s	0.000 s
On trigger jump to test end	no	no
Diagrams		

## Comment

## Test Module

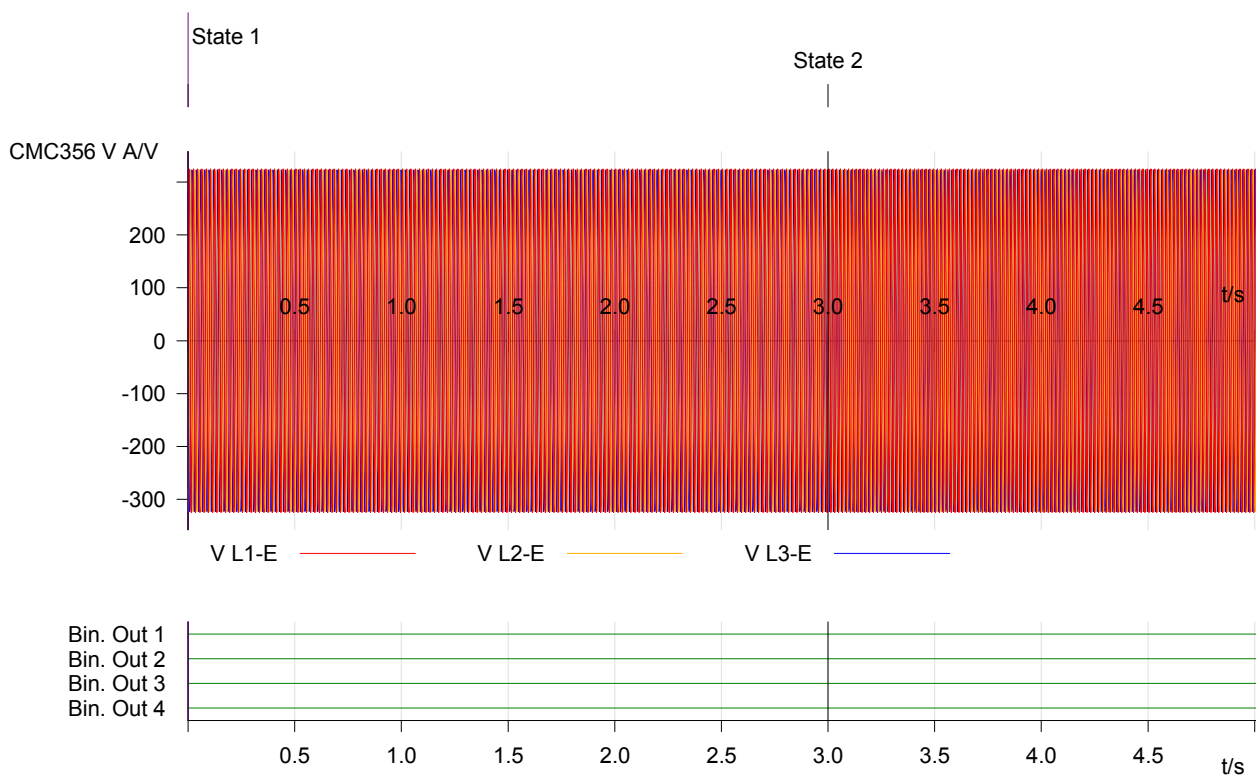
Name:	OMICRON State Sequencer	Version:	3.20
Test Start:	01-Dec-2017 11:13:33	Test End:	01-Dec-2017 11:13:39
User Name:	Dileepa	Manager:	Shanaka
Company:	Dara Switchboards		

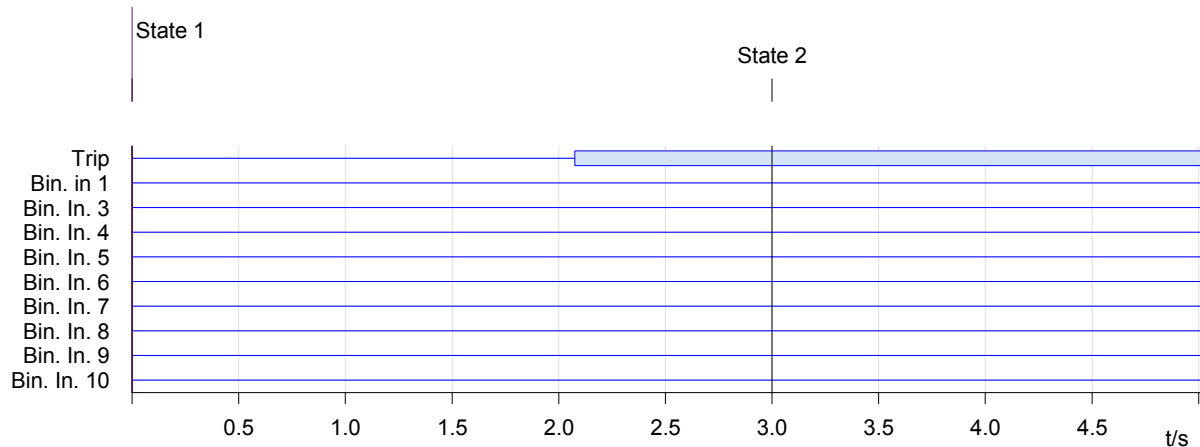
## Test Results

### Time Assessment

Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
O/F Time	State 2	State 2	Trip 1>0	2.000 s	100.0 ms	100.0 ms	2.011 s	10.90 ms	+

Assess: + ... Passed x ... Failed o ... Not assessed





### Cursor Data

	Time	Signal	Value
Cursor 1	0.000 s	<none>	n/a
Cursor 2	5.011 s	<none>	n/a
C2 - C1	5.011 s		n/a

### Event recorder

Time	Type	Signal name	Slope
2.076 s	Input	Trip	0>1
5.011 s	Input	Trip	1>0

Test State:  
Test passed

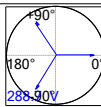
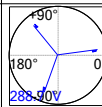
## Vector Shift Forward (78): Test Settings

### Ramp parameters

Outputs	Quantity	From	To	$\Delta$	TFault	TReset	Steps	Duration
V L1-E, V L2-E, V L3-E	Angle	7.00 °	10.00 °	0.50 °	3.000 s	3.000 s	7	47.00 s

### States

State	Reset State	Fault State
V L1-E	230.0 V 0.00 ° 50.00 Hz	230.0 V 0.00 ° 50.00 Hz
V L2-E	230.0 V -120.00 ° 50.00 Hz	230.0 V -120.00 ° 50.00 Hz
V L3-E	230.0 V 120.00 ° 50.00 Hz	230.0 V 120.00 ° 50.00 Hz
Bin. Out 1	0	0
Bin. Out 2	0	0
Bin. Out 3	0	0

Bin. Out 4	0	0
Diagrams		

### Test Conditions:

Start Test:	Immediately
Prefault time:	5.000 s
Stop ramp on assessment:	Yes
Delay after assessment:	0.000 s

### Fault Calculator:

Table Inputmode	Parameters				
Direct	V L1-E	230.0 V	0.00 °	50.00 Hz	
	V L2-E	230.0 V	-120.00 °	50.00 Hz	
	V L3-E	230.0 V	120.00 °	50.00 Hz	

### Comment

### Test Module

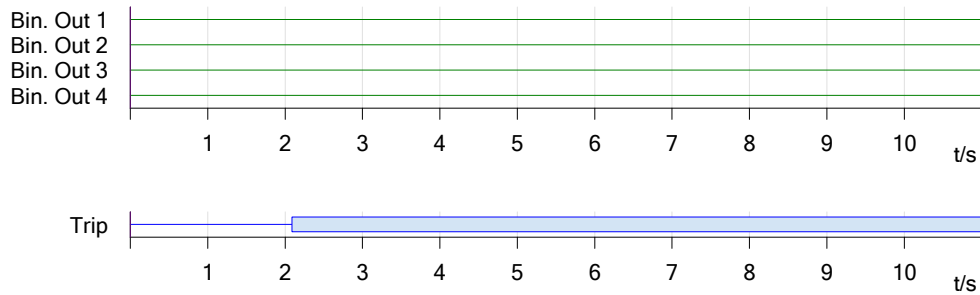
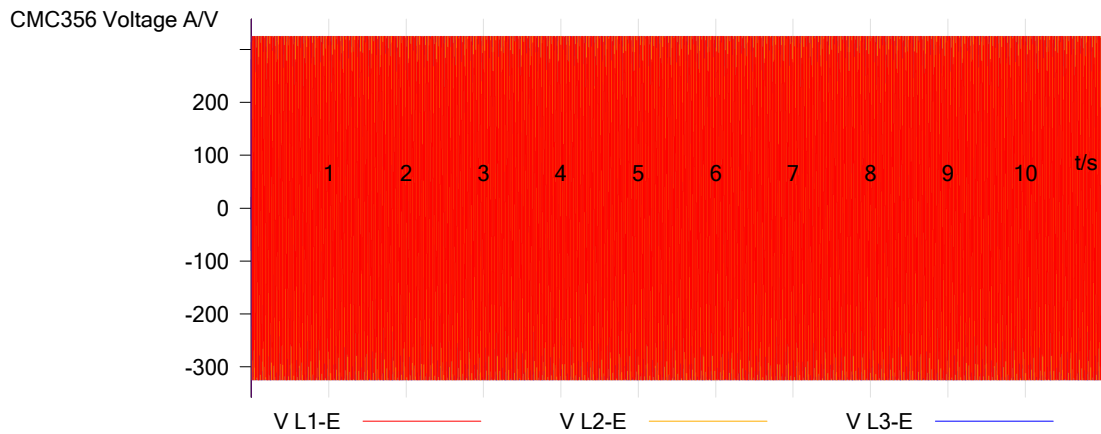
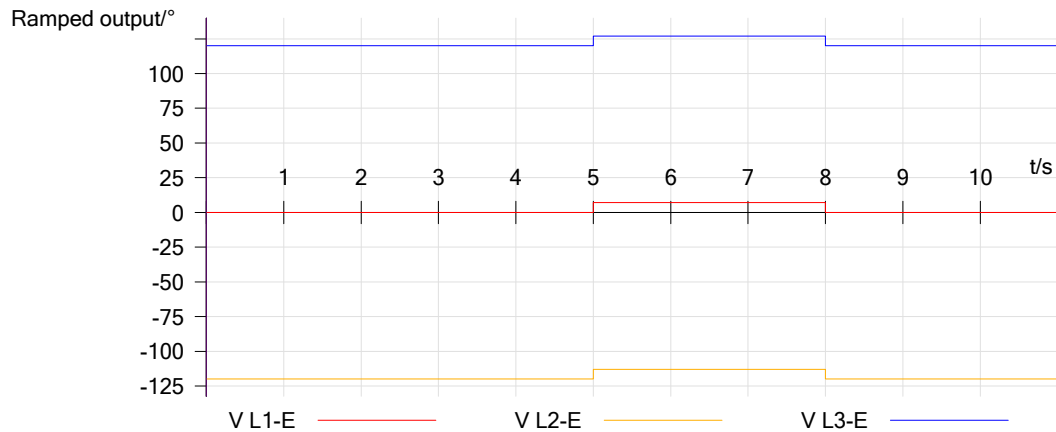
Name:	OMICRON Pulse Ramping	Version:	3.20
Test Start:	01-Dec-2017 11:14:12	Test End:	01-Dec-2017 11:14:26
User Name:	Dileepa	Manager:	Shanaka
Company:	Dara Switchboards		

### Test Results

Threshold	Assess on	Nom	Tol+	Tol-	Act	Dev	Assess
Phase angle V L1-E, V L2-E, V L3-E	Trip 1>0	8.00 °	1.00 °	1.00 °	7.50 °	-0.50 °	+

Assess: + .. Passed x .. Failed o .. Not assessed

Time at assessment: 97.60 ms



#### Cursor Data

	Time	Signal	Value
Cursor 1	0.000 s	<none>	n/a
Cursor 2	11.10 s	<none>	n/a
C2 - C1	11.10 s		n/a

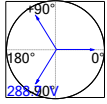
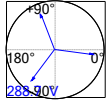
Test State:  
Test passed

#### Vector Shift Reverse (78): Test Settings

## Ramp parameters

Outputs	Quantity	From	To	$\Delta$	TFault	TReset	Steps	Duration
V L1-E, V L2-E, V L3-E	Angle	-7.00 °	-10.00 °	-0.50 °	3.000 s	3.000 s	7	47.00 s

## States

State	Reset State	Fault State
V L1-E	230.0 V 0.00 ° 50.00 Hz	230.0 V 0.00 ° 50.00 Hz
V L2-E	230.0 V -120.00 ° 50.00 Hz	230.0 V -120.00 ° 50.00 Hz
V L3-E	230.0 V 120.00 ° 50.00 Hz	230.0 V 120.00 ° 50.00 Hz
Bin. Out 1	0	0
Bin. Out 2	0	0
Bin. Out 3	0	0
Bin. Out 4	0	0
Diagrams		

## Test Conditions:

Start Test:	Immediately
Prefault time:	5.000 s
Stop ramp on assessment:	Yes
Delay after assessment:	0.000 s

## Fault Calculator:

Table Inputmode	Parameters			
Direct	V L1-E	230.0 V	0.00 °	50.00 Hz
	V L2-E	230.0 V	-120.00 °	50.00 Hz
	V L3-E	230.0 V	120.00 °	50.00 Hz

## Comment

## Test Module

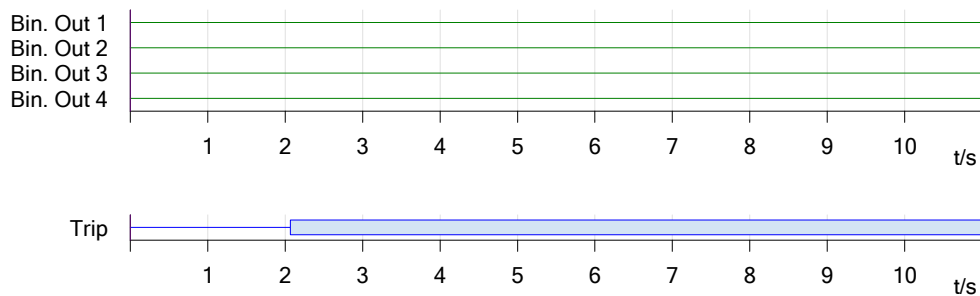
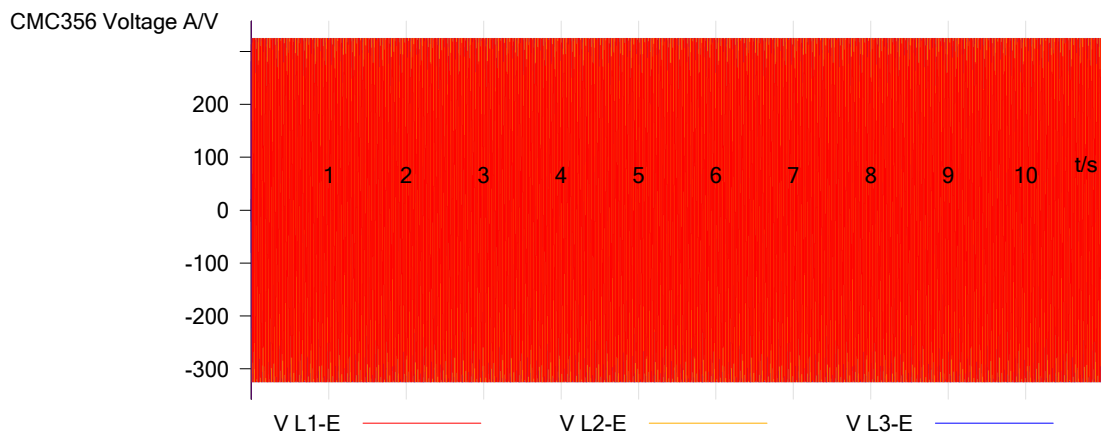
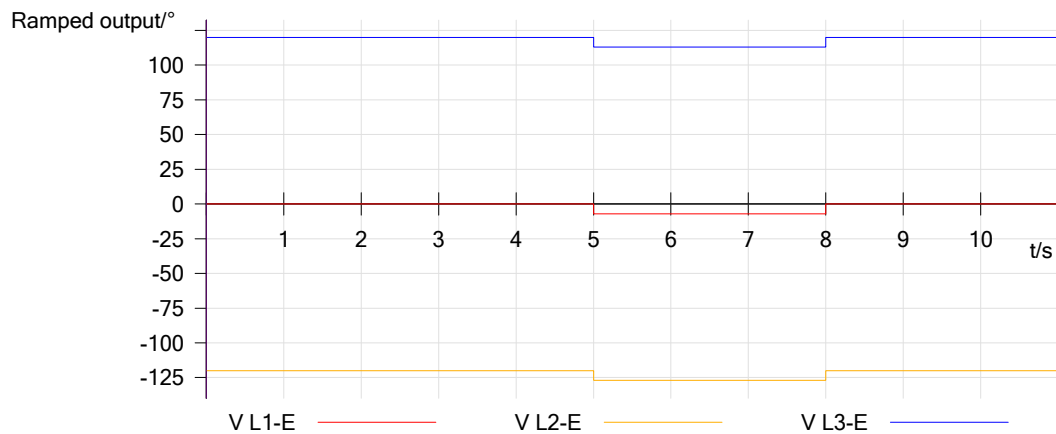
Name:	OMICRON Pulse Ramping	Version:	3.20
Test Start:	01-Dec-2017 11:14:56	Test End:	01-Dec-2017 11:15:10
User Name:	Dileepa	Manager:	Shanaka
Company:	Dara Switchboards		

## Test Results

Threshold	Assess on	Nom	Tol+	Tol-	Act	Dev	Assess
Phase angle V L1-E, V L2-E, V L3-E	Trip 1>0	-8.00 °	0.50 °	0.50 °	-7.50 °	0.50 °	+

Assess: + .. Passed x .. Failed o .. Not assessed

Time at assessment: 91.00 ms



#### Cursor Data

	Time	Signal	Value
Cursor 1	0.000 s	<none>	n/a
Cursor 2	11.09 s	<none>	n/a
C2 - C1	11.09 s		n/a

Test State:  
Test passed

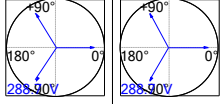
ROCOF (81R):  
Test Settings

Ramp parameters



Outputs	Quantity	From	To	$\Delta$	TFault	TReset	Steps	Duration
V L1-E,V L2-E,V L3-E	df/dt	1.500 Hz/s	2.500 Hz/s	100.0 mHz/s	2.000 s	5.000 s	11	82.00 s

## States

State	Reset State	Fault State
V L1-E	230.0 V 0.00 ° 50.00 Hz	230.0 V 0.00 ° 50.00 Hz
V L2-E	230.0 V -120.00 ° 50.00 Hz	230.0 V -120.00 ° 50.00 Hz
V L3-E	230.0 V 120.00 ° 50.00 Hz	230.0 V 120.00 ° 50.00 Hz
Bin. Out 1	0	0
Bin. Out 2	0	0
Bin. Out 3	0	0
Bin. Out 4	0	0
Diagrams		

## Test Conditions:

Start Test: Immediately  
 Prefault time: 5.000 s  
 Stop ramp on assessment: Yes  
 Delay after assessment: 0.000 s

## Fault Calculator:

Table Inputmode	Parameters			
Direct	V L1-E	230.0 V	0.00 °	50.00 Hz
	V L2-E	230.0 V	-120.00 °	50.00 Hz
	V L3-E	230.0 V	120.00 °	50.00 Hz

## Comment

## Test Module

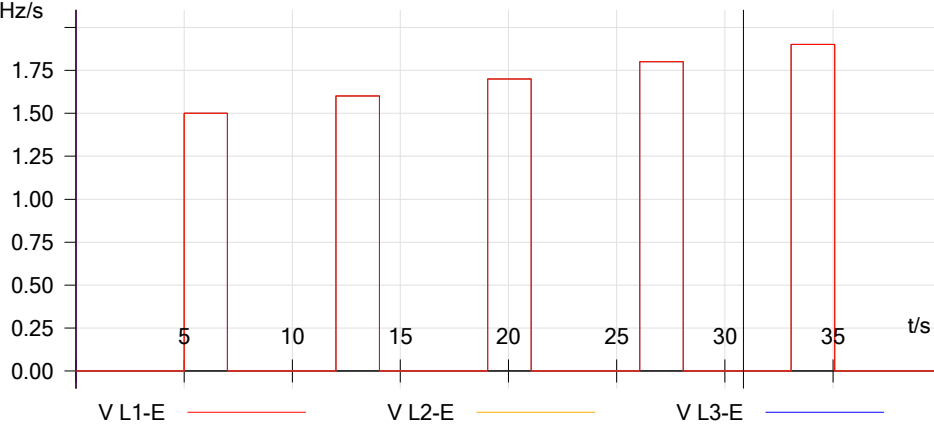
Name: OMICRON Pulse Ramping      Version: 3.20  
 Test Start: 01-Dec-2017 11:36:16      Test End: 01-Dec-2017 11:36:59  
 User Name: Dileepa      Manager: Shanaka  
 Company: Dara Switchboards

## Test Results

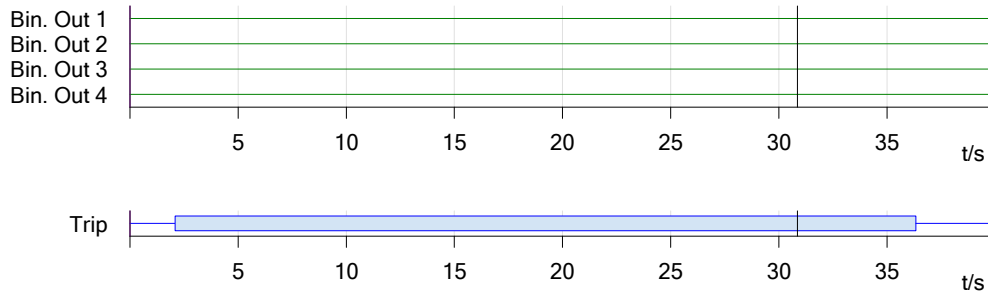
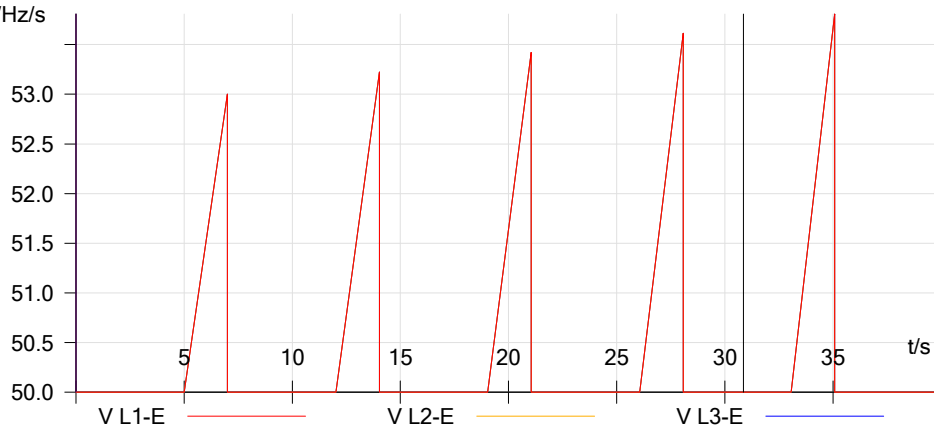
Threshold	Assess on	Nom	Tol+	Tol-	Act	Dev	Assess
df/dt V L1-E,V L2-E,V L3-E	Trip 1>0	2.000 Hz/s	200.0 mHz/s	200.0 mHz/s	2.000 Hz/s	0.000 Hz/s	+

Assess: + .. Passed   x .. Failed   o .. Not assessed  
 Time at assessment: 100.0  $\mu$ s

Ramped output/Hz/s



Frequency/Hz/s



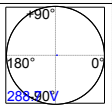
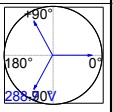
#### Cursor Data

	Time	Signal	Value
Cursor 1	0.000 s	<none>	n/a
Cursor 2	40.10 s	<none>	n/a
C2 - C1	40.10 s		n/a

Test State:  
Test passed

Re-connection Delay Time (s):

## Test Settings

State	State 1	State 2
V L1-E	0.000 V 0.00 ° 50.000 Hz	230.0 V 0.00 ° 50.000 Hz
V L2-E	0.000 V -120.00 ° 50.000 Hz	230.0 V -120.00 ° 50.000 Hz
V L3-E	0.000 V 120.00 ° 50.000 Hz	230.0 V 120.00 ° 50.000 Hz
Bin. Out 1	0	0
Bin. Out 2	0	0
Bin. Out 3	0	0
Bin. Out 4	0	0
Max. State Time	3.000 s	65.00 s
Trigger Logic		OR
Trip		1
User interaction	no	no
CMGPS trigger	no	no
IRIG-B/PTP trigger	no	no
Pulses / seconds	1	1
Delay after Tr.	0.000 s	5.000 s
On trigger jump to test end	no	no
Diagrams		

## Comment

## Test Module

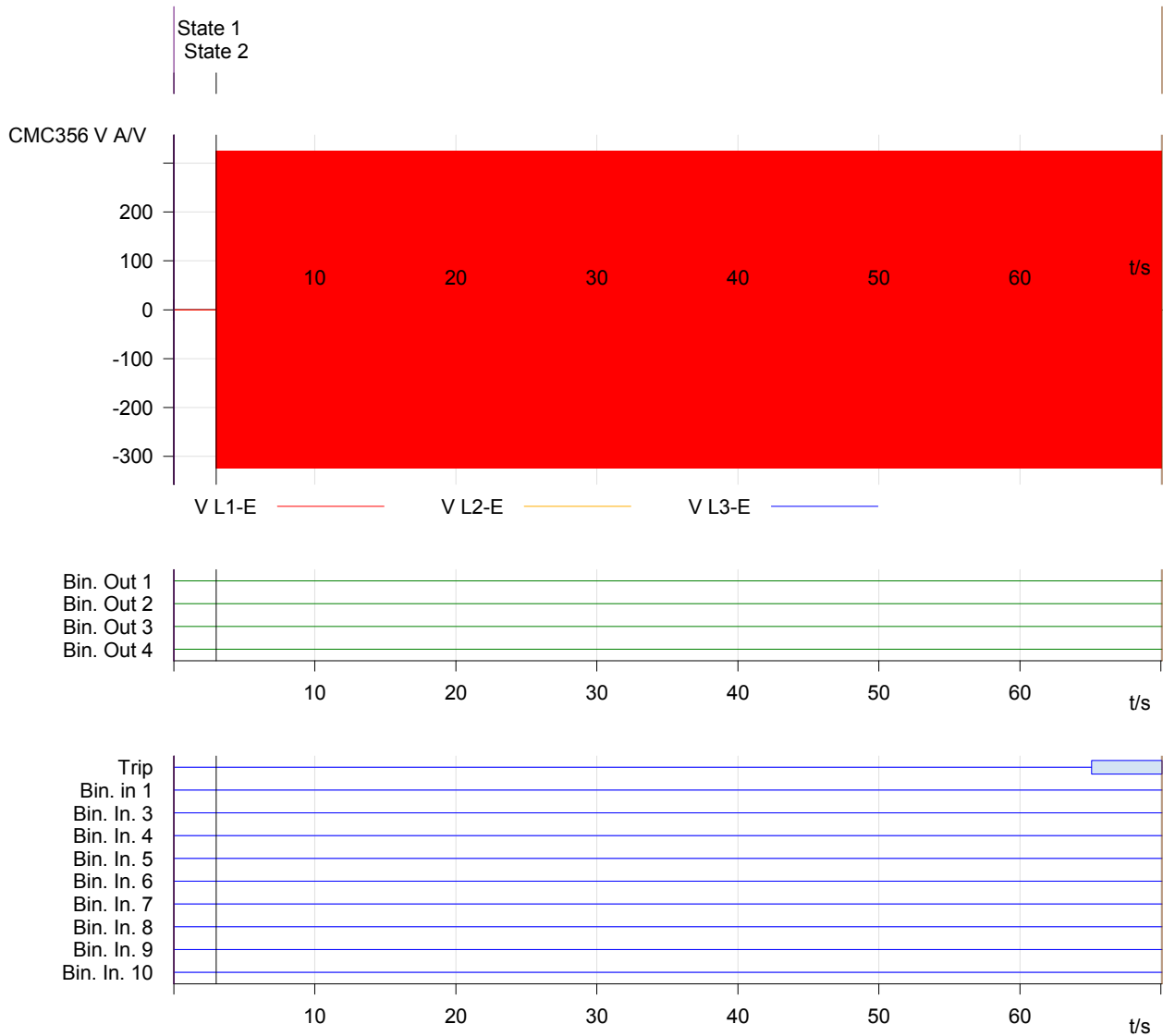
Name:	OMICRON State Sequencer	Version:	3.20
Test Start:	01-Dec-2017 11:45:50	Test End:	01-Dec-2017 11:47:02
User Name:	Dileepa	Manager:	Shanaka
Company:	Dara Switchboards		

## Test Results

### Time Assessment

Name	Ignore before	Start	Stop	Tnom	Tdev-	Tdev+	Tact	Tdev	Assess
Reconnection	State 2	State 2	Trip 0>1	62.00 s	2.000 s	2.000 s	62.08 s	80.80 ms	+

Assess: + .. Passed x .. Failed o .. Not assessed



### Cursor Data

	Time	Signal	Value
Cursor 1	0.000 s	<none>	n/a
Cursor 2	70.08 s	<none>	n/a
C2 - C1	70.08 s		n/a

### Event recorder

Time	Type	Signal name	Slope
65.08 s	Input	Trip	0>1

Test State:  
Test passed



**Head Office & Manufacturing Plant**

Brown – Denarusha Pty Ltd.  
5 Faigh Street  
Mulgrave, VIC 3170

TEL - (03) 8544 3300  
(03) 8787 5449

Email - [info@dara-switchboards.com.au](mailto:info@dara-switchboards.com.au)

**Dara Switchboards Express Production Plant (DEPP)**

28 Remount Way  
Cranbourne West, VIC 3977

**Dara Modular Switchboards Production Plant (DMPP)**

26 Remount Way  
Cranbourne West, VIC 3977