Local Droop Response Use Case

Core counts have been increasing steadily since IBM's debut of the Power 4 in 2001, eclipsing 100 CPU cores and over 1,000 for AI accelerators. While sea of processor architectures feature a stamp and repeat design, per-core workloads aren't always symmetrically balanced. For example, a cloud provider (AI or compute) will rent out individual core clusters to customers for specialized and varied workloads. However, this asymmetry combined with rapid provisioning changes can lead to localized voltage droops on the SOC resulting in potential logic glitches on cores running other workloads.

A localized voltage droop occurs when there is a sudden rush of switching activity, which creates a drop in the supply VDD and might raise the ground voltage level (also known as a ground bounce). A localized voltage droop might result in setup and hold time violations causing transient glitches and potentially catastrophic mission-mode failures.

System architects can respond to droops with adaptive clocking, which scales frequency down and up during voltage fluctuation. The technique requires a programmable clock and sometimes a droop detector. The latter can be optional if architects have deterministic workloads that can be managed with prior knowledge, which is rare for merchant silicon providers. Figure 1 shows how Movellus Aeonic Generate products can respond to a droop after VDD crosses the preset threshold. Design teams can reclaim Vmin margin reducing system power while maintaining or increasing system performance through adaptive clocking.

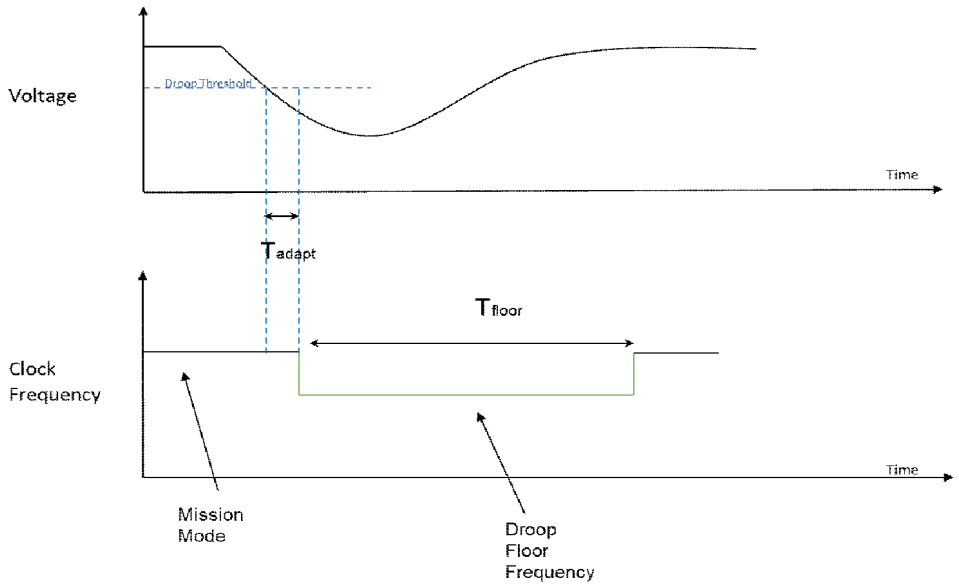

Figure 1. Example Timing and Voltage Profile of an Adaptive Clocking Solution

The Movellus Aeonic portfolio offers an adaptive clocking solution that delivers rapid droop response comprised of two building blocks: one providing adaptive clocking and the other providing droop detection. Together these building blocks mitigate localized timing glitches on the SoC. The Movellus Aeonic product portfolio is intrinsically flexible because it is built with synthesizable Verilog. Movellus' expertise lies in converting traditionally analog functions to digital, and this has allowed the company to develop feature-rich digital IP that is synthesizable. Synthesizable IP provides designers with configurable, scannable, and process-portable IP for a wide range of advanced SOC applications.

Figure 2 shows an example architecture of a sea of processor SoC with Aeonic Generate for localized droop support. An architect would pair an Aeonic Generate AWM module with a droop detector for the processor cluster and associated voltage domain to rapidly respond to workload-driven localized droops. This allows designers to deliver localized and independent droop response without altering the performance of neighboring processor clusters.

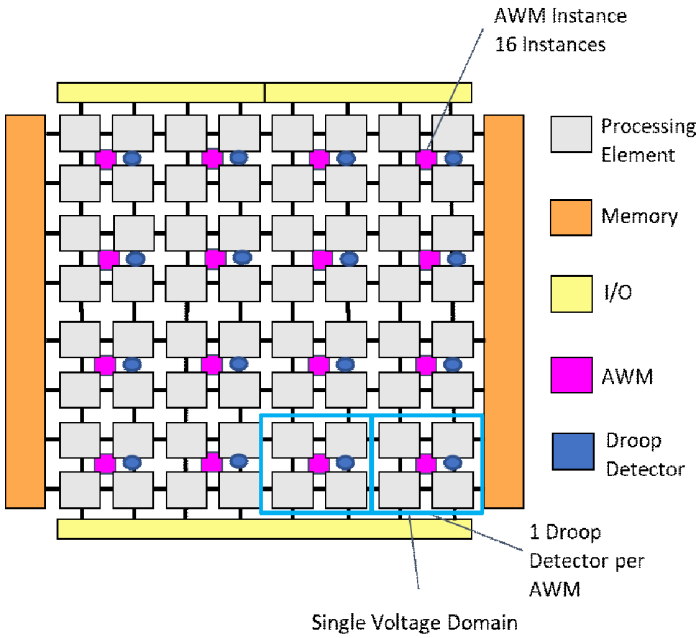

Figure 2. Example Sea of Processor SoC with Distributed Generate Modules for Local Droop Response

For distributed clock solutions, customers can integrate multiple Generate modules per chip to supply independently controlled frequencies to multiple compute cores. Being much smaller than traditional analog solutions, allows designers to easily instantiate the IP at the granularity required without any significant impact to the area. And as designs move to finer process geometries (e.g., 5 and 3nm), the Aeonic Generate area continues to scale - one of the many advantages of implementing clock generation digitally vs traditionally analog approaches.

As compute, inference, or training as a service continues to grow, silicon designers can improve system power and performance by quickly responding to localized droops. The Movellus Aeonic Generate family provides an adaptive clock generation solution that pairs rapid droop detection with near instantaneous frequency shifts - Droops happen, respond in time with Aeonic Generate.