Local Droop Use Case

Whether you serve the ADAS, PC, or networking market, chances are that your SoC is heterogeneous; containing general processing and application-specific accelerators. Your solution might have a systolic array for convolutions, a cluster of CPUs for application code, or a look-aside crypto engine for packet security. While application-specific accelerators significantly improve performance and power efficiency, they can face localized droops from dynamic workloads or induce droops under heavy load.

A localized voltage droop occurs when there is a sudden increase in switching activity driving an in-rush current, which creates a drop in the supply VDD and might raise the ground voltage level (also known as a ground bounce). A localized voltage droop might result in setup and hold time violations causing transient glitches and potentially catastrophic mission-mode failures.

System architects can respond to droop with adaptive clocking, which scales frequency down and up during voltage fluctuation. The technique requires a programmable clock and sometimes a droop detector. The latter can be optional if architects have deterministic workloads. Figure 1 shows how a clock generator will respond to a droop after VDD crosses the pre-set threshold. Design teams can reclaim the Vmin margin and raise system performance through adaptive clocking.

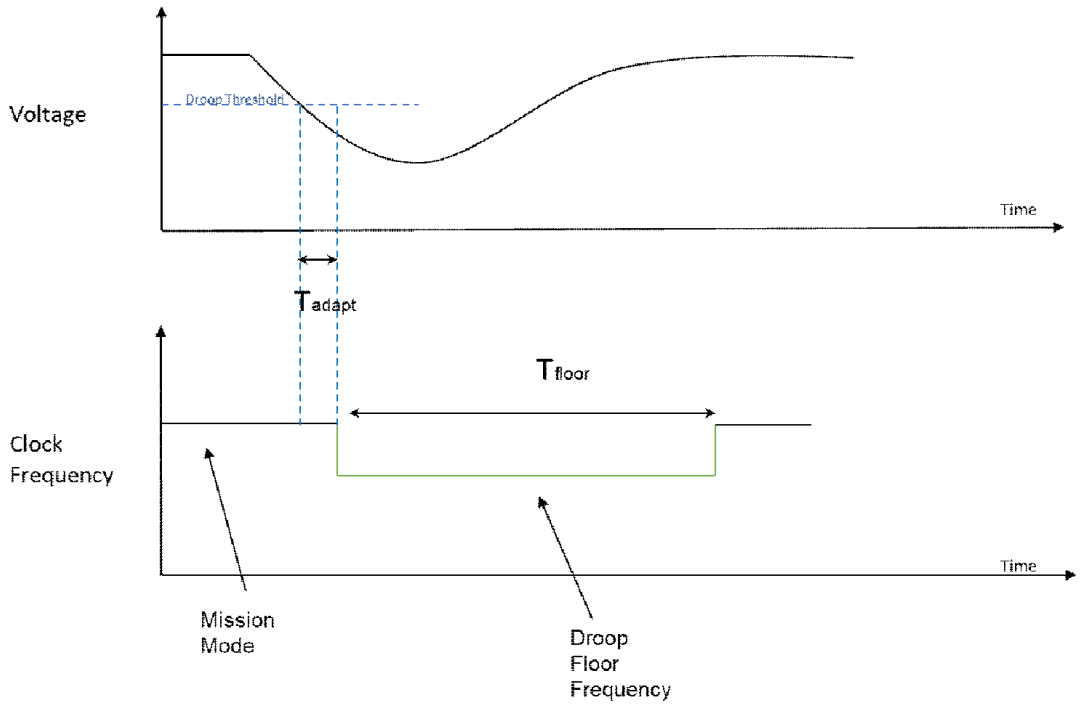

Figure 1. Example Timing and Voltage Profile of an Adaptive Clocking Solution

The Movellus Aeonic portfolio will offer an adaptive clocking solution that delivers rapid droop response comprised of two building blocks: adaptive clocking and droop detection. Together these building blocks mitigate localized timing glitches on the SoC. The Movellus Aeonic product portfolio is intrinsically flexible because it is built with synthesizable Verilog. Movellus' expertise lies in converting traditionally analog functions to digital, which has allowed the company to develop a synthesizable feature-rich digital IP. This provides designers with configurable, scannable, and process-portable IP for a wide range of advanced SOC applications.

Figure 2 shows an example architecture of an ADAS processor with the Aeonic Generate AWM Platform for localized droop support. An architect would pair an AWM module with an application-specific sub-block or accelerator to respond to workload-driven localized droops within five clock cycles with glitchless and rapid frequency shifts.

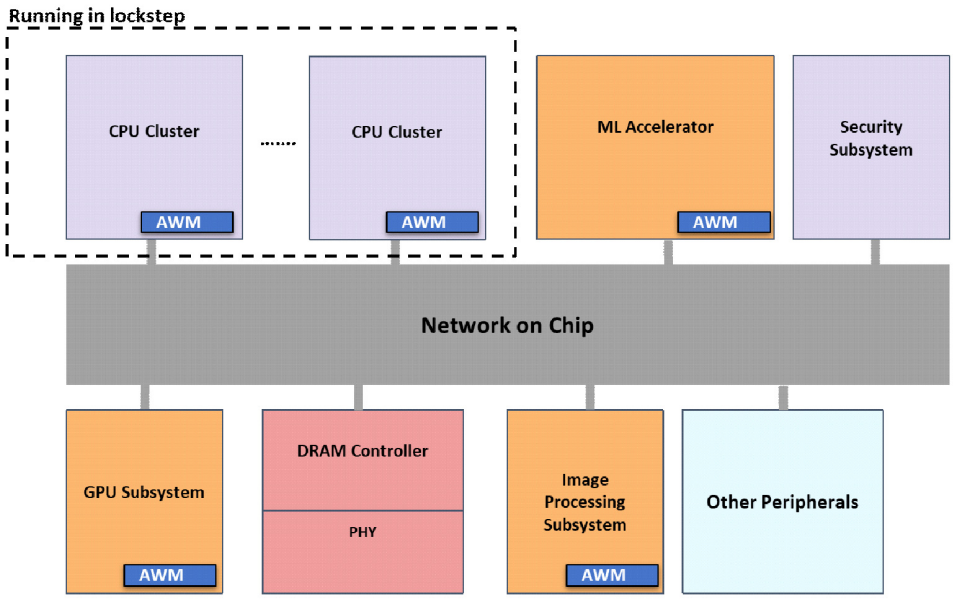

Figure 2. Example ADAS Architecture with Block-level Aeonic Generate AWM Integration

Application-specific domains deliver leaps in power and performance, and are necessary for comprehensive solutions in the ADAS, 5G, and data center networking markets. However, these same domains face varying workloads and utilization rates that lead to localized droops. Adaptive clocking solutions, such as the Aeonic Generate AWM Platform, swiftly respond to droop, resulting in more reliable performance with dynamic workloads. Droops will happen — respond in time with the Aeonic Generate AWM family.